Multiplexing Schemes and Equipment

Multiplexing Schemes

- FDM multiplexing schemes
- TDM multiplexing schemes
- Characteristics of the TDM hierarchy
- Characteristics of the military TDM hierarchies

TDM Equipment

- Equipment configurations and capabilities
- Terms and characteristics of the AN/FCC–100
- Terms and characteristics of the first-level multiplexer
- Characteristics of the AN/FCC–98
- Characteristics and functions of the second-level multiplexer
- Characteristics of the AN/FCC–99

This unit describes some of the various multiplexing schemes and equipment configurations that employ these techniques.

Multiplexing Schemes

A multiplexing scheme is nothing more than a plan for employing the various techniques we learned in our earlier lessons. These schemes are developed using frequency-division multiplexing (FDM), time-division multiplexing (TDM), or a combination of both (called hybrid systems). This section concentrates primarily on TDM schemes as they are predominantly what you encounter in the field. Before we get to TDM, however, let's discuss one example of a frequency-division multiplexing scheme.

FDM multiplexing schemes

The example we use here to explain FDM multiplexing schemes is the AN/UCC–4 multiplexer. This equipment used to be the standard frequency-division multiplexer used by the Defense Information Systems Agency (DISA). Although it is now outdated, the basic design and equipment functions still serve to describe how a FDM scheme is put together. It is not our intention to present detailed information on the AN/UCC–4, but we refer to it throughout this lesson when it applies to the subject.

The information provided by this text, when coupled with your on-the-job experience, will enable you to adapt to any FDM equipment scheme you may encounter. Foldout 1 (located in back of this volume) is a transmission equipment diagram for the AN/UCC–4, showing each major component required for processing a signal from the voice frequency (VF) channel level to the line frequency output. Although only one equipment shelf and tray of each type is shown, the diagram can be construed to represent a multiplex set of any channel capacity up to a maximum of 600 VF channels. Recall the

information we covered in FDM multiplexing techniques and refer to the foldout as we discuss the various FDM equipment components.

Envelope delay equalizer shelf. This section contains 12 plug-in modules; each module has a separate equalizer section for the transmit and receive circuits of one VF channel. The equalizer circuitry compensates for envelope delay distortion in one direction through the channel translating equipment. Most of this distortion occurs in the channel multiplexer and channel demultiplexer circuits and is the result of circuit component reactance in the channel bandpass filters.

Channel multiplexer shelf. The majority of the circuits required for each of the 12 VF channels are in two plug-in modules—a modulator and a bandpass filter. All the modulators are interchangeable and require only that a different carrier frequency be applied to each. The bandpass filter selects the lower sideband while suppressing all other modulation products.

The output of all 12 filters is combined across a hybrid transformer and applied to a balanced 135-ohm output circuit. Fifty of these channel multiplexers are required for a 600-channel system. Each channel multiplexer has an identical output of 60 to 108 kHz.

Group pilot injection shelf. The group pilot injection shelf performs two major functions for each of the five group transmitting circuits. One function is to insert a 104.08-kHz pilot into the 60- to 108-kHz group frequency band. The other function is to give the transmitting branch of the channel translating equipment a solid 135-ohm impedance at its output.

Each of the five group pilot injection shelves has two plug-in modules—a band elimination filter and an amplifier. As with the channel multiplexers, a 600-channel system requires a total of 50 group pilot injection shelves, one for each 12-channel group.

Group multiplexer shelf. The outputs of each of the five 12-channel groups are applied to a separate group modulator circuit and bandpass filter. The lower sideband products from the modulator are selected by a bandpass filter. The outputs of all five filters are applied to a hybrid transformer, where they are combined into a composite signal. The output frequency band of the composite signal is now 312 to 552 kHz. Ten group multiplexer shelves are required for a 600-channel system.

Supergroup modulator trays. For a 600-channel system, 10 supergroup modulator trays are required. Each supergroup modulator tray receives the 312- to 552-kHz output of the group multiplexer shelf and translates it to an assigned 240-kHz slot in the line frequency band of 60 to 2540 kHz. Each modulator tray consists of a plug-in modulator and two filters that are “hardwired” into the tray. The modulator tray for supergroup 2 provides no modulation and has a plug-in resistive pad in place of the modulator. This pad simulates the loss that the modulator would normally present to the signal.

Supergroup modulator combining panel. The supergroup modulator combining panel has facilities for combining the outputs of 10 supergroup modulator trays. The output frequencies of the 10 supergroups are combined across a hybrid transformer before they are applied to the line. Annulling networks ensure that the frequency response of the bandpass filters is flat throughout the entire filter bandwidth. These particular filters have been designed so that the reactance of one filter cancels or nullifies the reactance of an adjacent filter. This tends to keep the characteristic impedance of the filters across

the entire bandwidth resistive. All frequencies are offered the same amount of attenuation.

When the multiplexer set is configured for less than 600 channels, annulling networks are put in place of the bandpass filters that are not used. These networks present the proper amount of reactance to the active filters. A synchronizing pilot tone can be added to the composite signal and used at the receive terminal to synchronize the carrier frequencies of both terminals.

Supergroup demodulator combining panel. The modulator and demodulator combining panels have similar circuits; the main difference is the signal flows through in opposite directions. A 96-kHz bandpass filter selects the synchronizing pilot tone from the line frequency band, 60 to 2540 kHz, and applies it to the carrier generation circuitry. The line frequency band is then applied to a total of 10 supergroup demodulator trays by a hybrid transformer.

Supergroup demodulator trays. Each supergroup demodulator tray translates one of the supergroup line frequency bands to the basic supergroup band of 312 to 552 kHz. A separate tray is used for each supergroup, and with the exception of supergroup 2, they all function in the same way. There is no demodulator for supergroup 2, as the only circuit needed is a bandpass filter to select the 312- to 552-kHz band from the line frequency. One of the main differences between the supergroup demodulator and the supergroup modulator is the requirement for amplifiers.

Group demultiplexer shelf. The group demultiplexer shelf demultiplexes the 312- to 552-kHz frequency band into five separate 60- to 108-kHz frequency bands. The function of the group demultiplexer shelf is the same as the group multiplexer shelf except that the process is in the reverse order.

Group pilot alarm shelf. The group pilot alarm shelf performs two major functions for each of the five groups in the receive circuits. One function is to monitor the 104.08-kHz group pilot and give an alarm if the pilot varies 5 decibels (dB) above or below the normal signal level. The other function is to provide isolation and impedance matching between the group distribution frame and the output of the group demultiplexer shelf.

Channel demultiplexer shelf. The channel demultiplexer shelf demultiplexes the 60- to 108-kHz frequency band into 12 separate 300- to 3400-Hz VF channels. It also provides a means of amplification and level adjustment for each VF channel.

These components of the AN/UCC–4 multiplex set are the major circuits through which the signal flows during the modulation and demodulation processes. These particular circuits are essentially the same in any other frequency-division multiplexer. The component nomenclature and the physical arrangement of the equipment racks may be different, but the basic multiplexing and electronic principles are the same.

TDM multiplexing schemes

There are two basic modes of operation for time-division multiplexing: those that repeatedly assign a portion of time to each channel and those that assign time slots on an as-needed basis. The first form is referred to as Synchronous Time-Division Multiplexing (STDM). The “as-needed” form of TDM is referred to as Asynchronous Time-Division Multiplexing (ATDM) or Statistical Time-Division Multiplexing (Stat-Mux). To differentiate in this text, TDM, when we use it without a leading name (i.e., asynchronous or statistical), refers to the synchronous variety. Although the majority of

this text is dedicated to synchronous TDM, we cover a brief discussion of statistical TDM first.

Asynchronous TDM (Stat-Mux). Statistical TDMs operate with framing formats that are basically identical to synchronous framing formats. The major difference is that a Stat-Mux system periodically redefines the length of its frames to change the number of time slots and, hence, the number of channels. Whereas a synchronous system permanently assigns a time slot to each of its channels, a Stat-Mux system assigns a time slot *only* when a channel becomes active. A time slot is eliminated (the frame shortened) when the respective channel becomes inactive. This technique can greatly increase the capacity of the multiplexer since time slots are only used for active channels.

When the actual traffic is far below the potential traffic in a STDM system, most of the time slots on the output are wasted. Consequently, it is impossible to use an output line with less capacity than the sum of the input lines. A Stat-Mux system can do this using an arrangement called *concentration.* The usual approach is to only transmit actual data and not dummy characters (as STDM would have done). However, this strategy introduces the problem of telling the receiver which character came from which input line. One solution to this problem is to send two output characters for each input character; the channel number and the data.

Unfortunately, concentration has an inherent difficulty. If each channel suddenly starts outputting data at its maximum rate, there is insufficient capacity at the output to handle it all. Some data may be lost. For this reason, concentrators are always provided with extra buffers (memory space) in order to survive short duration data surges. This is only the tip of the iceberg when it comes to statistical multiplexing. We cover them in more detail when we discuss digital networking later.

Synchronous TDM. Synchronous TDM is an arrangement whereby individual channels take turns utilizing a single transmission path. This is made possible by using a technique called *sequential sampling.* In sequential sampling for TDM, the channels are always sampled in the same order; that is channel 1 is always sampled in a time slot that may be designated time slot 1, channel 2 in time slot 2, channel 3 in time slot 3, and so on.

When all of the channels, up to the capacity of the multiplex equipment, are sampled in succession, the sequence begins again. The sequences, referred to as *frames*, repeat themselves at a fixed rate that is the same as the channel sampling rate. Sequential sampling of channels in this manner is called *interleaving* and is the basis for the framing structure generated. Interleaving for four channels carrying analog signals is illustrated in figure 3–1.

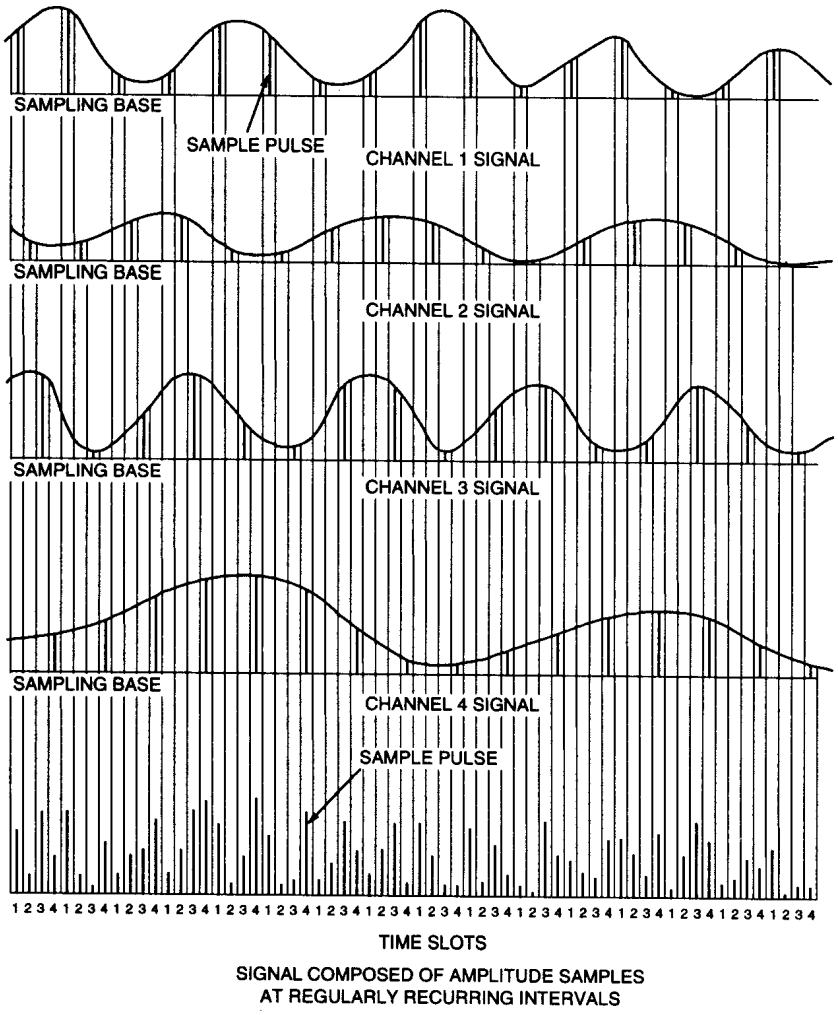

Figure 3–1. Interleaving of amplitude samples for time-division multiplexing.

Since pulse-code modulation (PCM) employs periodic sampling, it is used as a basis for time-division multiplexing of analog signals. A pulse-code modulator samples a number of analog channels in sequence and encodes the samples in the same sequence (fig. 3–2). The process is known as PCM-TDM.

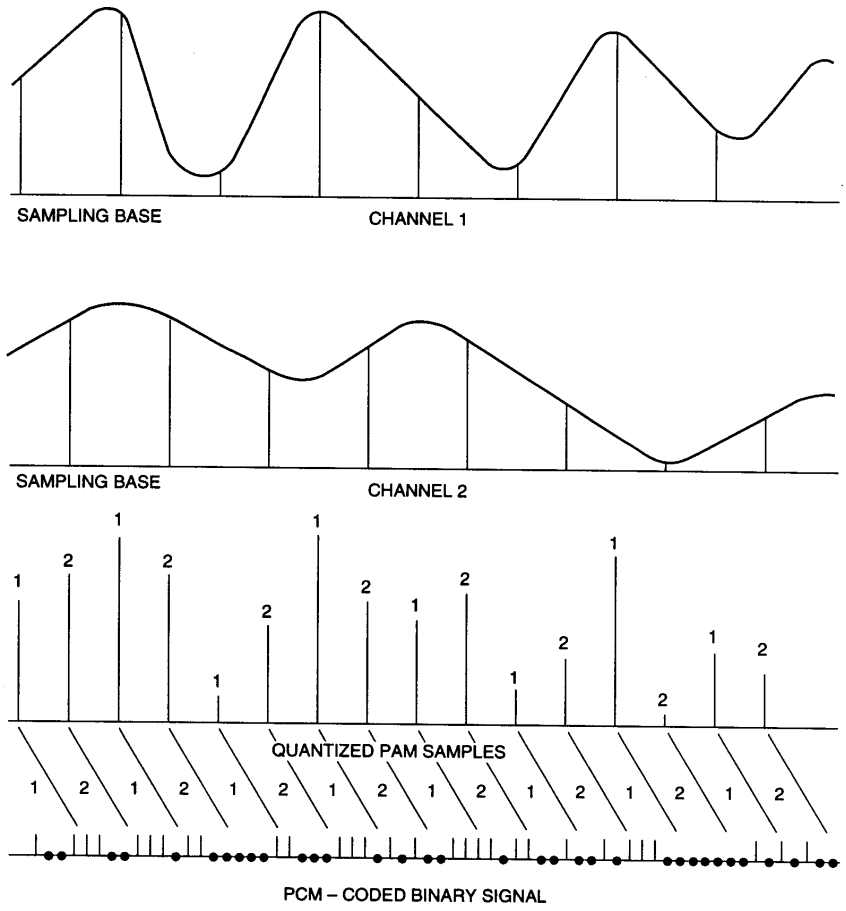

Figure 3–2. Formation of binary signal in PCM-TDM.

Binary signals can be brought to the TDM sampling rate by buffering and pulse-stuffing techniques (to be explained later in this lesson) and interleaved directly. Other digital data signals may be sampled in the same manner as analog signals. However, it is necessary to convey the timing of transitions accurately; otherwise, the data signals cannot be reconstructed faithfully.

Accuracy can be provided by sampling at a high enough rate. The higher the rate, the smaller is the interval in which the transition can be defined and, hence, the more precisely its time of occurrence can be conveyed. Sampling rates, however, must be limited to the capabilities of the transmission system. Often, these rates are too low for accurate sampling of transition times.

Framing. As covered previously in this volume, PCM-TDM code words from a number of channels are arranged into sequences, or frames. All pulse streams resulting from TDM must be formatted into frames. This means that the binary digits representing signals from a number of sources must be combined serially in a periodic manner. The pulse sequence from one period (or a fixed number of periods) is identified as a frame. The resulting binary signal structure is referred to as the *line format.* Its purpose is to enable the receiving equipment to sort out the incoming pulses and assign them to the proper channel (synchronization).

One method of framing involves inserting a unique pattern of digits known as the *framing pattern.* The pattern may consist of alternating 1s and 0s, but other patterns have been found optimal in PCM systems. There are three methods of inserting framing bits for synchronization. The pattern may be transmitted for a consecutive stream of bits at the beginning or at the end of a frame or may be distributed throughout the frame. The three arrangements are shown in figure 3–3.

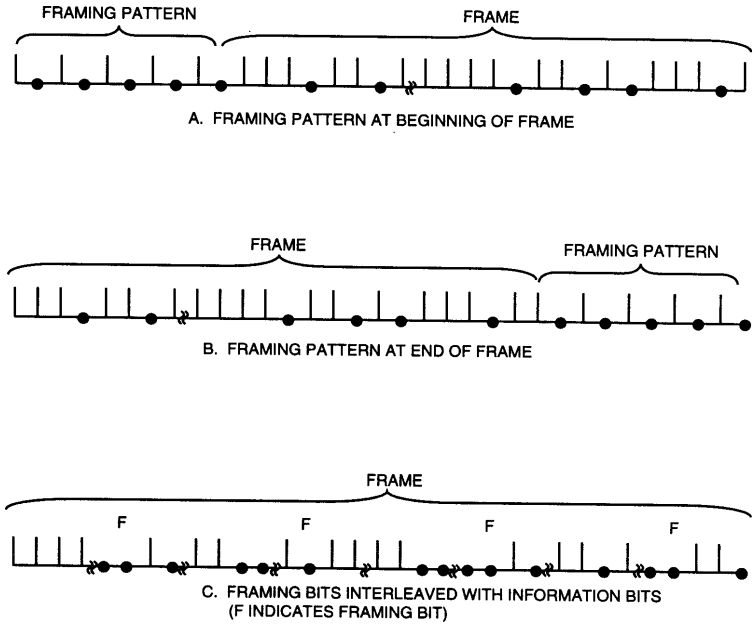

Figure 3–3. Transition coding and sampling of digital data signal for TDM.

Whatever pattern and transmission sequence is used, the receiving equipment is designed to generate the same pattern and sequence by comparing the received bit patterns with its internally generated pattern until it detects the matching pattern. It then locks onto the pattern, thereby identifying the framing of the received bit stream. This technique is known as added bit framing.

As a general rule, the longer the framing pattern, the greater is the probability of maintaining the in-frame condition over communications circuits that are impaired by significant noise levels. Framing patterns of 10 bits and longer have been found to offer the least mean time to acquire or re-acquire framing. The more bits we use for framing, however, the less we have for information. A good compromise is to limit the number of framing pattern bits to 0.05 times the total frame bits. Thus, a framing pattern of 15 bits would be used for a 300-bit frame.

To minimize the time required to acquire or re-acquire framing, it is permissible to accept some bit errors in the framing pattern. This introduces the possibility of incorrect framing by locking onto a false pattern. Thus, a tradeoff is required between the probability of accepting a false pattern and the longer acquisition time required if only a

completely correct pattern is acceptable. In system design, this tradeoff becomes a factor in equipment selection.

There are several different framing structures in use. They vary primarily in the order that channels are sampled and in the number and code combination of the framing bits used. Since it is impossible to cover all the possible structures, we use a standard 24-channel format for explanation purposes. This is the format used by the Department of Defense in the first-level multiplexers used in the Digital European Backbone (DEB) system. Some information presented here merely summarizes and reinforces the techniques we already learned by showing them in practical application.

Using the 24-channel format, one sample from each channel plus one framing bit is considered a frame and a group of 12 frames constitutes a superframe. Each frame contains one synchronizing (framing) bit so that the receiving terminal can decode, demultiplex, and distribute the incoming bit stream properly. When examined as a superframe, extracting one framing bit from each frame forms a 12-bit sequence. This sequence is used for frame synchronization and for telephone (control) signaling information. The basic framing bit pattern simply alternates between a one (1) and a zero (0) for each successive frame. This pattern is followed as long as no control signaling is required. When control signaling is present, the sequence is altered for that superframe.

Each frame consists of 24 words (one per channel) plus a framing bit. Since each channel is sampled in sequence at a rate of 8000 times per second (Nyquist sampling theorem), 8000 frames per second are produced, with a framing bit being inserted between channel 24 and channel 1. Each of the channel words consists of 8 bits that are presented serially to the bit stream. Since there are 24 channels, a frame consists of 192 data bits (24 x 8) plus 1 framing bit or 193 bits total. Since there are 8000 frames produced per second, the output bit stream is 1.544 Mb/s (193 bits/frame x 8000 frames/second).

The 8 bits of each channel word may represent PCM voice or straight digital data. If the word represents voice, then control signaling may be transmitted as well as the voice signal. This is done by time-sharing the least significant bit (8th) of every sixth frame on the 8-bit amplitude coding systems or by using the 8th bit all the time on older model channel bank systems (such as the D1). When digital data are used, the signaling bit time-sharing is *inhibited.* Thus, the full 8-bit word is available for data.

Synchronization. While framing identifies the recurring sequences of signal samples, thereby providing the starting points for the sorting out of individual signals on reception, the bits comprising the sequences must be interleaved at precise time intervals to identify the signals they represent. Timing by an electronic clock provides the basis for interleaving at precise intervals. The signal from the clock is a continuous series of regularly spaced pulses. These pulses are the sampling pulses used by the TDM process.

Digital signals coming into TDM equipment from a number of channels have no deliberate timing relationship with each other. The channels may originate at different distances from the multiplexing point, the signals may travel by different transmission media, and they could vary over a period of time. Such differences and variations preclude an arrangement whereby multiple signals would arrive in precise time relationship with each other—a requirement for TDM.

TDM also requires that the receiving end of a multiplexed link operate with the same timing as the sending end. Timing differences can lead to incorrect decoding of the bit stream. Timing differences can arise from (1) slight variations in operating rates at the two ends of the circuit and (2) variations in propagation delay over the circuit.

Synchronization is the solution to both problems. Incoming channels to the TDM equipment must be synchronized with each other and with the multiplex timing. Both ends of a TDM circuit must be synchronized with each other. Before we get too far ahead, let's define the three basic types of synchronization: (1) asynchronous, (2) synchronous, and (3) isochronous.

Asynchronous. This is a system in which the performance of each operation is dependent on the traffic that contains the timing signals, where each stage of the operation *recovers clock* from the traffic signal. An example of this is the Baudot telegraphy code where the stop pulse of the "character or frame" has a longer time interval.

Synchronous. In a synchronous system, the performance of all operations is controlled by a *master clock.* Synchronization of the system is independent of the traffic passing on the channel or system concerned. This method has the distinct advantage of allowing up to 25 percent more bits to be transmitted than asynchronous signals do, because the use of parity bits is eliminated.

Isochronous. The third type of synchronization, which you may or may not be familiar with, is isochronous. With this system the data signals are passed *without timing* (clock) and without character framing bits such as the start-stop bits used in asynchronous signals. The term "isochronous" means equal time. That is, each bit is equal in time to each other bit. All bits are the same length, as opposed to the type of signal used in start-stop systems, where the stop bit may be longer than the other bits. This type of synchronization is usually seen in "higher level" multiplexing techniques to conserve bandwidth and maintain signaling speed efficiencies. These synchronization methods are covered in some aspects later.

Timing. The basis for synchronization is timing. Timing generators, referred to as *clocks,* are used at both ends of digital circuits. The clock on the receiving end of a circuit is made to keep time with the clock on the transmitting end in some manner. The receiving clock, however, must be made to lag the transmitting clock to allow for the time required for the signal to transmit from the transmitting to the receiving end; this is referred to as the *propagation delay.* The delay is subject to variation. Furthermore, the transmitting clock itself exhibits some variation. Consequently, special measures are required to provide the correct timing on the receiving end.

Master clock. One clock in a system can be designated the master clock, and all other clocks are slaved to it. This requires a separate timing circuit just to carry the timing signal from the master clock to the slaved terminals.

Synchronization pulses. Another method adds a synchronizing pulse to each grouping of information pulses in a manner similar to that used in the start-stop telegraphy described earlier. This method wastes transmission capacity, since it replaces some information bits with synchronizing pulses.

Pulse stuffing. Pulse stuffing is a technique for synchronizing digital signals coming into TDM equipment over paths of different and varying delay

characteristics. It is also used to adapt low-speed digital signals for transmission over higher speed facilities. Pulse stuffing depends on the outgoing digital rate of the multiplexer being higher than the sum of the incoming rates. The incoming pulse streams are stuffed with the right numbers of pulses to raise their rates to the local single-channel rate. When a sampling interval at the local rate coincides with a space between pulse intervals in an incoming pulse stream, a pulse is generated at the sampling interval. This is a stuffed pulse. Information on the time of occurrence of the stuffed pulses is transmitted to the receiving equipment so that the pulses can be removed on reception.

Figure 3–4 illustrates the pulse stuffing and the corresponding destuffing. The figure assumes multiplex equipment operating at an outgoing line rate that is a multiple of 4800 bits per second (b/s). An incoming pulse stream at approximately 4200 b/s is pulse stuffed to the 4800-b/s rate prior to multiplexing (fig. 3–4,A). The demultiplexed 4800-b/s signal at the receiving end is destuffed to the original rate (fig. 3–4,B).

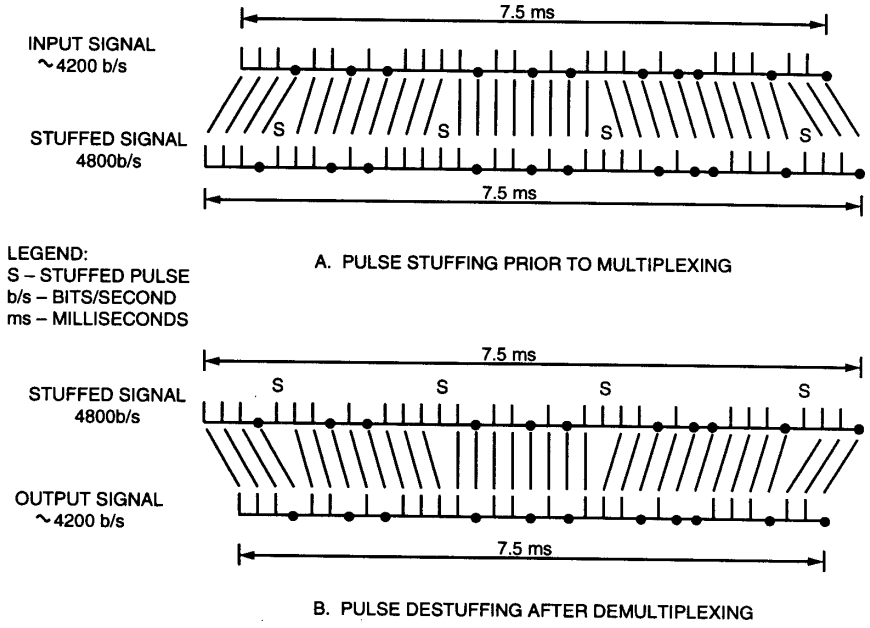

Figure 3–4. Pulse stuffing of a signal for TDM.

Characteristics of the TDM hierarchy

Before we progress any further, you should have a thorough understanding of the TDM hierarchy. This is a very important concept to you simply because of the nature of your job as a systems controller. When you are troubleshooting a communications outage, you must be "system orientated," which means looking at the entire picture rather than looking for a single piece of defective equipment or single part of the communications link. Once you have completed your localized in-house troubleshooting, you must understand your transmission media's hierarchy to determine your next step in isolating the cause of the outage.

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Meaning of hierarchy. Like the frequency translation of an FDM signal, TDM stages follow a progressive organization called a *hierarchy.* Figure 3–5 is a simple hierarchy illustrating how each progressive stage interleaves numbers of channels from the preceding stages, resulting in progressively higher data rates. The first company to develop and effectively use this type of systems control was the Bell System. The components of the Bell System hierarchy are channel banks (PCM-TDM), multiplexers (TDM), and lines. This hierarchy is shown in figure 3–6.

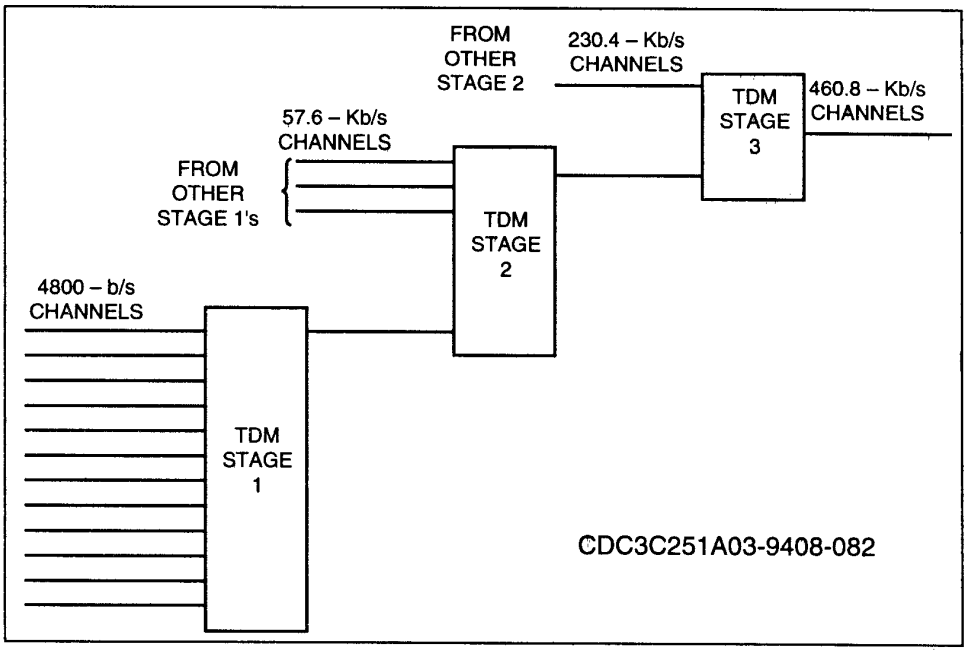

Figure 3–5. Progressive stages of time-division multiplexing.

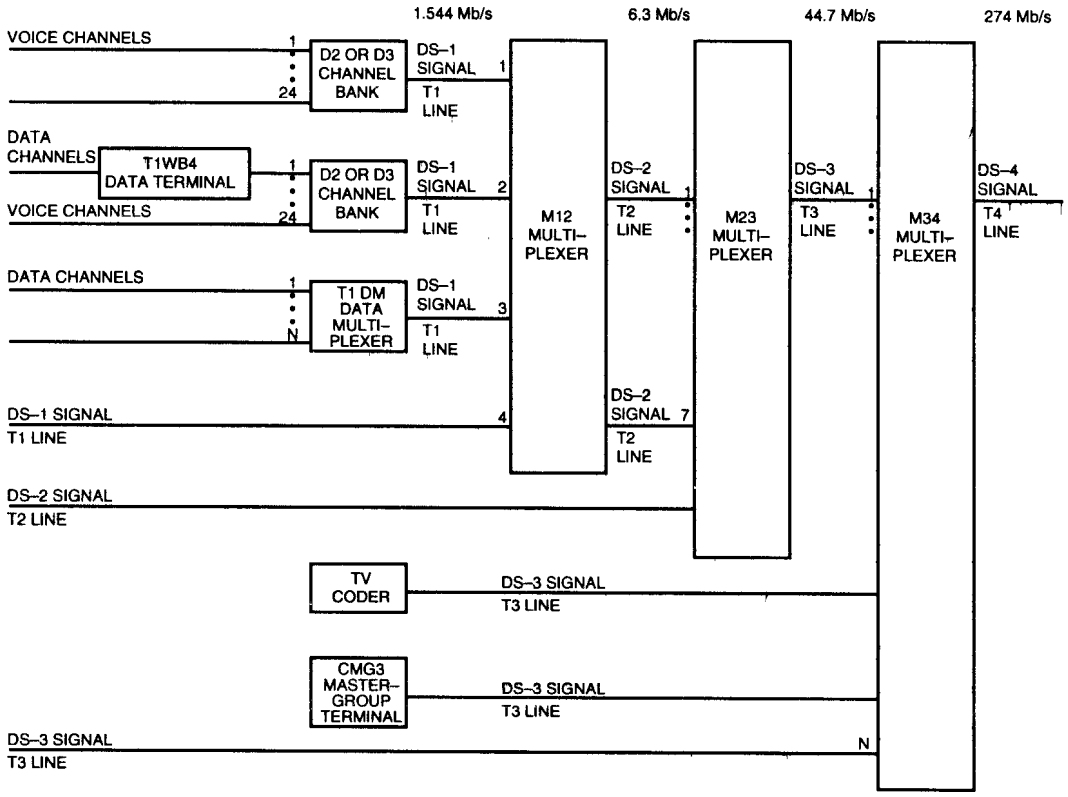

Figure 3–6. Bell System TDM hierarchy.

Channel banks. The Bell System established the digital TDM hierarchy which is the basis for military and commercial systems alike. In figure 3–6 we refer to the Bell System PCM-TDM channel banks by their Western Electric equipment nomenclature. This system provides for three channel bank designations: D1, D2, and D3.

The D1 channel bank converts 24 analog voice channels into PCM channels and formats the bits into frames. Each voice channel sample is encoded into a 7-bit binary code word. An eighth bit is added to each code word for signaling and supervision purposes. Each channel is sampled at a rate of 8 kHz; thus the PCM channel rate is 64 kb/s (8000 samples per second times 8 bits per sample). One frame of 24 voice channels consists of 192 bits (8 bits per sample times 24 channels sampled in one frame). A synchronization bit is added to each frame, giving a total of 193 bits per frame. The corresponding transmission speed is 1.544 Mb/s (8000 frames per second x 193 bits per frame). The Bell System designation for a 1.544-Mb/s signal is DS–1, and communication lines operating at this rate are termed as T1.

The D2 and D3 channel banks were designed to be T1 compatible; that is, the output bit stream of these channel banks is at the 1.544-Mb/s rate. Both use the entire 8-bit code word of a PCM channel for quantizing the voice signal, which results in an improved *signal-to-quantizing-distortion ratio.* Recall from a previous lesson that an 8-bit code provides 256 possibilities, whereas the 7-bit code used in the D1 channel bank provides only 128.

Signaling in the D2 and D3 channel banks can no longer be accommodated by the eighth bit of each code word, since all eight bits are assigned to quantizing steps. Hence, the eighth bit of the code word for each channel must be “robbed” frequently to carry the signaling and supervision information. The system has been standardized to use the eighth channel bit every sixth frame.

The D3 channel bank offers the advantages of both D1 and D2 channel banks and is compatible with both. The only differences occur in channel sampling and alarm sequencing.

Data channels can be interleaved with PCM voice channels in any of the D channel banks by using a T1WB4 data terminal to enter the data channel into the D channel bank. The data signals are inserted in 8-bit bytes.

Data channels can replace PCM voice channels in a DS–1 signal. When all the input channels are data channels, a T1DM data multiplexer is used instead of one of the D channel banks.

Higher level multiplexers. The Bell System multiplexers that combine data signals at levels above DS–1 are designated by the levels they bridge. Multiplex M12, for example, time-division multiplexes four DS–1 signals into a DS–2 signal. The levels being bridged are 1 and 2. Multiplexer M23 combines 28 DS–1 signals into a DS–3 signal. Multiplexer M34 combines six DS–3 signals into a DS–4 signal. This is illustrated in figure 3–7. The signal data rates are not exact multiples of the lower level signals being multiplexed since framing and other control bits must be added. A DS–2 signal has a rate of 6.312 Mb/s; a DS–3, 44.746 Mb/s; and a DS–4, 274.176 Mb/s. According to Bell System designations, a T2 line carries the DS–2 signal; a T3 line, the DS–3 signal; and a T4 line, the DS–4 signal.

Digital Signal Number	Number of Voice Circuits	Multiplexer Designation	Bit Rate (Mbps)	Transmission Media
DS–1	24	D channel bank (24 analog inputs)	1.544	T1 paired cable 1A radio(DUV)
DS–1C	48	M1C (2 DS–1 inputs)	3.152	T1C paired cable
DS–2	96	M12 (4 DS–1 inputs)	6.312	T2 paired cable
DS–3	672	M13 (28 DS–1 inputs)	44.736	3A–RDS 11–GHz radio
DS–4	4032	M34 (6 DS–3 inputs)	274.176	T4M coax WT4 waveguide DR18 18 GHz radio

Figure 3–7. Digital TDM Signals of North America and Japan.
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For military applications, digitized voice and data channels are provided by time-division multiplexers. Usually data channels are provided by a three-level multiplex hierarchy as illustrated in figure 3–8. Referencing the illustration, D–1 data channel service is provided by a Voice Frequency Carrier Telegraph (VFCT), or similar equipment. The low-speed time-division multiplexer (LSTDM) is used to interface with low-speed data circuits (point D–2) and to time-division multiplex them into data trunk groups (usually at 56 kb/s).

The data trunk groups and medium-speed data users are provided digital channels by the AN/FCC–98 (point D–3). These data channels are multiplexed into digroups (1.544 Mb/s—point D–4) along with voice signals that have been digitized using pulse-code modulation (PCM). These digroups are multiplexed by multiplexers such as the AN/FCC–99 into mission bit streams at 3.232, 6.464, 9.696, and 12.928 Mb/s for internodal transmission. We cover the characteristics of these TDM equipment types in later lessons.

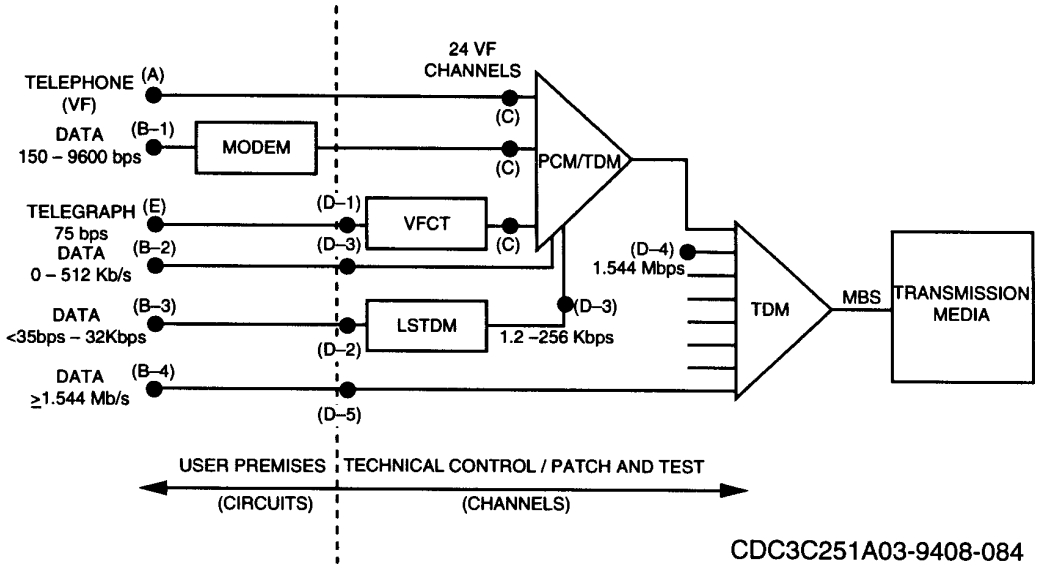

Figure 3–8. Basic equipment configuration.

Because many circuits and trunks used in the military systems transverse both FDM and TDM equipped transmission systems, you should become familiar with the standards that have been established for them.

Characteristics of the military TDM hierarchies

There are two basic military TDM hierarchies of interest in this lesson: the flexible hierarchy used in the Digital European Backbone (DEB) and the DCS hierarchy used as the basis for Digital Radio and Multiplex Acquisition (DRAMA). Both share compatibility with the Bell System T1 at the first-level TDM.

DEB system. The DEB system uses the AN/FCC–98 to provide first-level multiplexing for up to 24 channels (1.544 Mb/s). The second-level multiplexer used is the AN/FCC–(99), which interfaces up to eight AN/FCC–98 inputs (192 channels) and has an output data rate of 12.928 Mb/s. Third-level multiplexing is performed by the AN/FRC–(171)(V) microwave radio set which interfaces two AN/FCC–99 inputs.

DRAMA program. The equipment included in the DRAMA program represents a standardization of the DEB system. First-level multiplexing is done in the FCC–98 channel banks; and the second level, in the AN/FCC–99. A third level of multiplexing is provided in the microwave radio. The DRAMA TDM hierarchy is the same as the DEBs and is shown in figure 3–9.

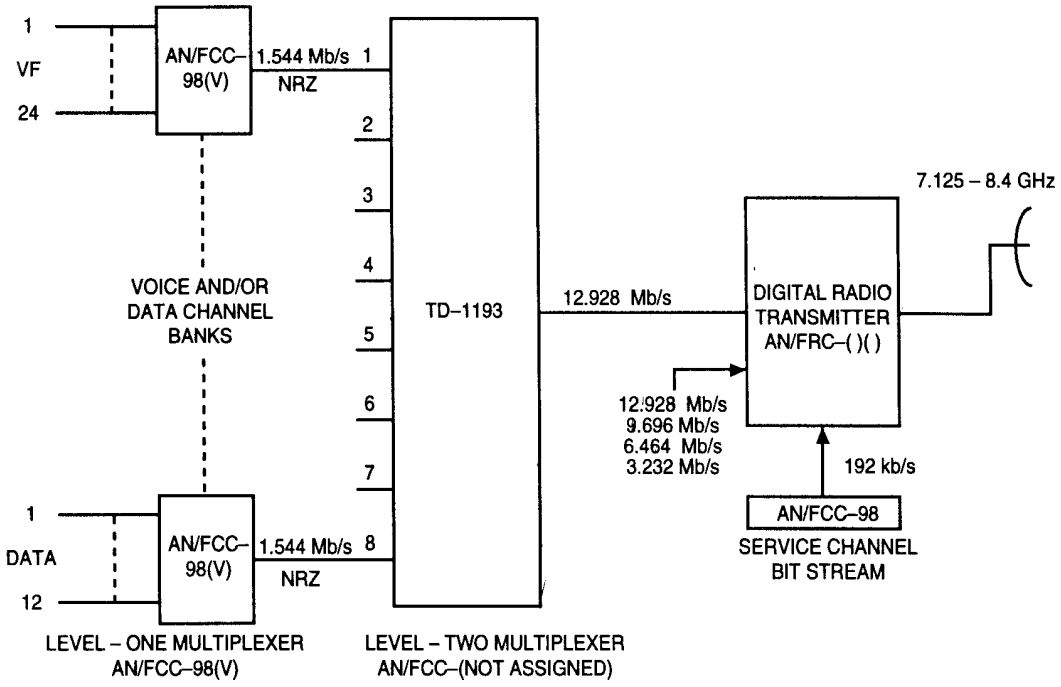

Figure 3–9. Digital European Backbone and DRAMA TDM hierarchy.

CCITT hierarchy. The hierarchy recommended by the International Telephone and Telegraph Consultative Committee (CCITT) is based on first-level multiplexing and PCM with one of two optional output data rates: 1.544 Mb/s or 2.048 Mb/s. The lower rate is the same as the T1 rate, but the framing and synchronization patterns are different. The higher rate accommodates 30 voice channels instead of the 24 of the lower rate (figure 3–10). Most of the world, except the United States, Canada, and Japan, is starting to use the higher rate. The difference between the North American standards and the CCITT recommendations will ultimately preclude worldwide standardization of digital communications.

Level Number	Number of Voice Circuits	Multiplexer designation	Bit Rate (Mbps)
1	30		2.048
2	120	M12	8.448
3	480	M23	34.368
4	1920	M34	139.264
5	7680	M45	565.148

Figure 3–10. Digital TDM Hierarchy of CCITT.
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TDM Equipment

In this section we cover some of the common equipment that is used to multiplex voice and data signals into a composite data stream for transmission over the DCS. For simplicity the explanation is directed toward the AN/FCC–100 LSTDM, the 24-channel mode of the AN/FCC–98 first-level multiplexer, and the AN/FCC–99 second-level multiplexer.

Equipment configurations and capabilities

The rapid growth of digital communications has resulted in a proliferation of time-division multiplexing schemes produced by different manufacturers. To achieve the standardization required in large-scale communications, the military services and major telecommunications common carriers and administrations have concentrated on a limited number of systems composed of the available TDM components. Some of the predominant TDM systems are listed in figure 3–11. The listing also indicates the multiplex level, which is simply the number of TDM stages accommodated by the system.

Description	Remarks	Multiplex level	Commercial off-the-shelf	Tri-service
AN/FCC–97	Consists of two T1–400s	2	–	X
TD–1192	Also AN/FCC–98	1	–	X
TD–1193	Used in DRAMA Also AN/FCC–99	2	–	X
VICOM T1–4000	Two used in AN/FCC–97	2	X	X
AN/FCC–98	Used in LDRAMA and TD–1192	1	–	X
AN/FCC–99	Used in DRAMA	2	–	X
AN/FCC–100		Sub	–	X
TD–1220(V)/G	1–12 data channels; operates at –48VDC pwr	1	–	X
TD–1226(V)/G	Same as TD–1220, except operates at 115VAC	1	–	X
TD–968	US Army specified	1	–	X
AN/GSC–24(V)	1–15 data channels	1	–	X
D1, D2, D3	Bell System channel banks	1	X	–
M1–2	Bell System, T1 to T2	2	X	–
Lendurt 9120A	Duobinary coding output	2	X	–
TSEC/CY–104	Consists of D2 channel bank plus encryption function and interface unit	1	–	X
OB–79(V)1/FSC	Also VICOM T1–4000	2	–	X

Figure 3–11. Predominant TDM Systems.

There are many different manufacturers of TDM equipment and you are probably familiar with or have heard of some of the types of equipment listed in figure 3–11. The following equipment descriptions state some minimum performance capabilities.

Microwave radio set. The radio equipment must be capable of transmitting 192 PCM voice channels, which is 12.6 megabits per second (Mb/s) data, over line-of-sight (LOS)

links in a 7-MHz bandwidth and 384 PCM channels (252 Mb/s data) in a 14-MHz bandwidth. This represents 1 b/s per Hz of bandwidth bit-packing efficiencies at 7 MHz and 2 b/s per Hz of bandwidth bit-packing efficiencies at 14 MHz. The specific configuration requirement depends on the channelization and frequency allocations currently being processed.

First-level multiplexer. The first-level multiplexer (channel bank) combines up to 24 voice channels using PCM. Data channel capability is also provided on a VF channel replacement basis with bit rates (0 to 20 kb/s, 50, 56, 64, and 128 kb/s) in accordance with the DISA system performance specification. The military first-level multiplexer is intended to provide a common channel bank for the DSCS (satellite) and DCS (terrestrial) applications with a 3-, 6-, 12-, and 24-channel capability.

Second-level multiplexer. The second-level digital multiplexer accepts up to eight T1 (1.544 Mb/s) data streams and multiplexes the T1 lines (ports) into a single high-speed data stream. The term "T1 data stream" means a data stream of 1.544 Mb/s, while a "port" is an input, an output, or a test point.

COMmunications SECurity (COMSEC) equipment. The first-level primary multiplexing and bulk encryption is sometimes done through the use of cryptographic (termed "crypto") equipment. The crypto unit must be capable of accommodating 50 kb/s ±500 b/s asynchronous data streams within any of the PCM voice channels on a plug-in channel unit replacement card basis, except in the 24th channel, which integrates the framing function for the multiplex. The crypto unit is used to assemble 24 VF channels or 23 50-kb/s data channels, or some mixture of these, into a bulk-encrypted 1.544-Mb/s digital stream for insertion into a port of the second-level multiplex. Bulk encryption can be done after the first-, second-, or third-level multiplexing or at all of these levels with the TSEC/KG–81. The TSEC/KG–81 can accommodate the 192,384, and 768 kb/s as well as 1.544-Mb/s data rates associated with the 3/6/12/24 channel operation of the AN/FCC–98 first-level multiplexer.

Supervisory subsystem. System order wires are incorporated into the digital message baseband. The maintenance coordination circuit, the fault alarm, and status reporting (FASR) channel are multiplexed into a composite baseband and operate independently of the message baseband or mission multiplex.

Terms and characteristics of the AN/FCC–100

The AN/FCC–100 is a low-speed time-division multiplexer (LSTDM) with full-duplex transmit and receive capabilities. The AN/FCC–100 operates at speeds up to 256 kb/s and provides 16 ports capable of handling any mix of synchronous, asynchronous, and isochronous (transitional encoded) data transmission. The AN/FCC–100 is configured at the user's location to specific communication system requirements.

Downline loading capability permits an operator to configure a remote AN/FCC–100 from a centrally situated unit. This capability eliminates the need for an operator at a remote location during reconfiguration. Once installed and configured, the AN/FCC–100 is capable of performing multiplexing, demultiplexing, timing, control, synchronization, framing, monitoring, and alarm reporting.

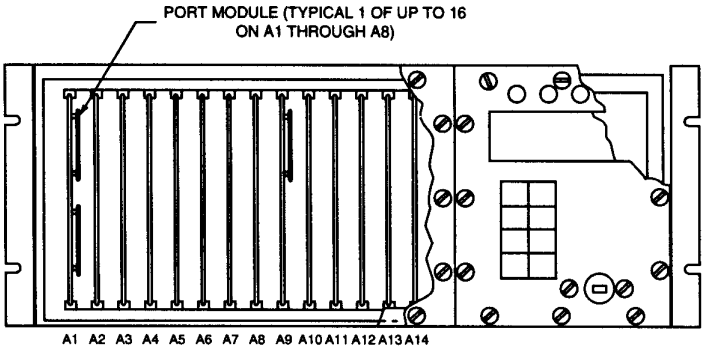
Timing for the AN/FCC–100 is provided by a highly accurate internal oscillator or from an external timing source. Data loopback capabilities and plug-in, modular design further

enhance diagnostic and repair capabilities of the AN/FCC–100. If required, troubleshooting and corrective maintenance to the module replacement level is accomplished on-site while the AN/FCC–100 is in place.

The AN/FCC–100 is capable of both sending and receiving data, voice, and signaling information in the form of a single mission bit stream (MBS). This mission bit stream (referred to as the "aggregate") is capable of handling up to 16 separate channels. A time-division principle is employed to place all channels onto a single synchronous aggregate.

The individual channels are determined by selection of interchangeable plug-in port modules. The aggregate is determined by selection of interchangeable plug-in aggregate modules. Once selected, the port and aggregate modules are configured by the operator. The output signal of the AN/FCC–100 is then connected to a single port of a first-level multiplex such as the AN/FCC–98.

Modules. The AN/FCC–100 and its port modules are illustrated in figure 3–12. The following is a brief description of these modules.



NOTE:
MODULE ACCESS PANEL REMOVED

POSITION	MODULE
A1 THROUGH A8	PORT CARRIER
A9	AGGREGATE CARRIER (WITH AGGREGATE MODULE)
A10	TRANSMIT PROCESSOR
A11	RECEIVE PROCESSOR
A12	SHARED LOGIC
A13	BITE
A14	INTERFACE

Figure 3–12. AN/FCC–100 port modules.

Transmit processor module. This module contains the logic circuitry and memory devices that are required to send user data to the aggregate. The module also performs some diagnostic checks.

Receive processor module. This module contains the logic circuitry and memory devices that are required to accept user data from the aggregate. The module also performs most of the diagnostic checks associated with built-in testing.
Shared logic module. This module contains the circuitry that is required by both processor modules. The memory circuits that contain both active and off-line configurations are located on this module.
BITE module. This module contains comparator circuits and light emitting diode indicators (LEDs), which are used to monitor specific voltages and clock signals. A test probe can plug into this module. The probe is used to monitor test points on the other modules.
Port carrier modules. These eight modules contain the circuitry common to receiving data from, and sending data to, user terminals. Each module can support up to two ports.
Aggregate carrier module. This module contains the circuitry required to send data to, and receive data from, the aggregate. It requires a specific aggregate module to provide the driver circuits.
Interface module. This module permits communication between the user and the AN/FCC–100. The module converts operator inputs into commands that configure and control the AN/FCC–100. It also converts signals from the AN/FCC–100 into output displays.

Terms and characteristics of the first-level multiplexer

To fully explain the operation of the first-level multiplexer we need to review and expand on the TDM process. The theory of operation of the PCM equipment is adapted from the *Lenkurt Demodulator* and available technical orders. Permission to use materials from Lenkurt Demodulator is gratefully acknowledged.
Theory of operation. Our objective is to trace a signal from entry into the system to its reconstruction at the distant end. This hypothetical system is very similar to the DEB and DRAMA systems.
First-level multiplex (PCM channel bank). The first operation is to sample the speech signal at a suitable rate and to measure the amplitude of the signal at the time of sampling. This operation is equivalent to pulse-amplitude modulation (PAM). Refer to foldouts 3 and 4.
Sampling. It has been proven mathematically that, if a continuous electrical signal is sampled at regular intervals at a rate of at least twice the highest significant signal frequency, the samples contain all of the information of the original signal. This principle is known as the sampling theorem. A continuous signal waveform, therefore, can be represented completely if at least two amplitude samples are transmitted for each cycle of the highest significant signal frequency.
Ordinarily, in a PCM system designed for speech signals, we use a sampling rate of 8000 Hz, or one sample every 125 microseconds (1/8000 seconds) as covered in our previous discussions.
Quantizing. Sampling a continuous speech signal at regular intervals results in a series of pulses, the voltage amplitudes of which are proportional to the level of the signal at the time of sampling. The amplitudes may be at any of an infinite number of values within the intensity range of speech. The usual intensity range encountered in telephone systems is about 60 dB, or a voltage ratio of 1000 to 1.

After sampling, the next step in the PCM process is to divide or quantize the 60-dB intensity range into increments or amplitude levels to permit binary digital coding. These discrete levels, known as quantum steps, represent any level within the speech range by using the quantum step nearest to the actual amplitude value of the pulse sample. For example, assuming that quantum step 8 equals 8 volts and quantum step 9 equals 9 volts, an actual amplitude sample with a value of 8.24V would be represented by quantum step 8. A sample value of 8.61 would be represented by quantum step 9, etc. Refer to foldout 5. Channel 4 PAM sample reached a level of +84 and the binary code is equal to 11010011.

Encoding. If each quantum step is numbered in decimal form, then some type of digital code can be developed to represent each of the numbers. Ordinarily, a binary code that consists of a combination or code group of binary 1s and 0s is used, each group representing a decimal number.

The number of quantum steps that can be represented with a binary code is 2^n, when "n" is the number of binary digits (or bits) required in each code group. Therefore, a 5-bit code is required for 32 (or 2^5) quantum steps, while a 7-bit code is needed for 128 (2^7) steps. In systems using a 7-bit code, the speech amplitude range is normally divided into 127 quantum steps. Step 64 is ZERO reference, with 63 steps positive and 63 steps negative. For our example (refer to foldouts 4 and 5), we have selected an 8-digit code (2^8) using 256 quantum steps. The first digit assigns the polarity; 1 is positive, while 0 is negative. (Zero sample values code as positive or negative, since the polarity bit is a two-level signal and cannot assume a neutral state.)

Referring to foldout 5, you can see that the PAM bit for channel 1 has a level of –66V. This converts to a binary code of 01000010. If the level had been –65.75V, the code would have been the same. However, if the level had been –65.3V, the code would be 01000001, because the level would be rounded to the nearest quantum step, which is 65.

In some cases, the quantum step only approximates the actual value. There is always some error. The maximum error is equal to one-half the size of the quantum step. In speech signals, such errors are random and cause what is usually referred to as quantizing error or noise. Quantizing noise is the major source of signal distortion in PCM systems. The level of quantizing noise is mainly a function of the number of quantum steps used. When the number of quantum steps is increased, the quantizing noise decreases. Since an increase in quantum steps results in a narrower pulse, the bandwidth required to transmit the coded signal is increased.

Each sample in the PCM pulse train is now in the form of an 8-bit non-return-to-zero (NRZ) word. The data is processed through an encryption device and then through an interface device. The interface device changes the NRZ data to bipolar data, which is fed to one port of the second-level multiplexer.

One example of a first-level multiplexer is the AN/FCC–98.

Characteristics of the AN/FCC–98

The AN/FCC–98 multiplexer, which is a first-level multiplexer, uses analog-to-digital conversion (A/D) PCM techniques to multiplex and demultiplex voice-frequency signals for transmission over a digital communications system. It has the capability of

multiplexing/demultiplexing 3, 6, 12, or 24 voice channels and also has the capability of multiplexing input data rates of 0 to 20 kb/s, 50 kb/s, 56 kb/s, 64 kb/s, 128 kb/s, 256 kb/s, and 512 kb/s.

Pulse-code modulation used by the AN/FCC–98 involves transforming continuously variable speech signals into a series of digitally coded pulses and then reversing the process to recover the original analog signals. This is accomplished in three steps.

The first operation is to *sample* the analog signal in each voice channel and measure the amplitude of the signal at each sampling time, which is similar to pulse-amplitude modulation (PAM). Second, the voltage amplitude of each sample is assigned to the nearest value of predetermined discrete voltages, which is *quantizing.* To improve the signal-to-quantizing distortion, small quantizing steps are used for large samples. We explained this *nonuniform quantizing* process earlier. The third and final step is *encoding,* where a digital code is assigned to each discrete amplitude value.

Each voice channel in the AN/FCC–98 is sampled, quantized, and encoded in sequence every 125 microseconds (1/8000 seconds), or at a sampling rate of 8 kHz. Eight-bit encoding is used; therefore, there is a total of 2^8 or 256 quantizing steps.

The eight bits of each channel word may represent PCM voice or digital data. Supervisory signaling, (on-hook and off-hook), control signaling, (dial pulses), and information signaling (dial tones, ring-backs, etc.) must be transmitted, as well as the voice samples. This is done by time-sharing the least significant bit (B8) between voice and signaling (fig. 3–10). The B8 bits of each voice channel carry voice sample information for five frames, followed by one frame of signaling information. This is followed by five more frames of B8 voice and another frame of B8 signaling. This sequence is repeated every 12 frames. Even though this technique uses one of the voice digits (the least significant bit), it does not affect the quality of the voice transmission through the channel. When data channels are used, the signaling bit time-sharing of B8 is inhibited.

This 8-bit code word makes up one word. With a sampling rate of 8 kHz and 8-bit encoding, 64 kb/s is required per voice channel. The time slots that make up one 125-microsecond period (one 8-bit word from each of the 24 channels) constitute a frame. Figure 3–13 shows the word and frame format.

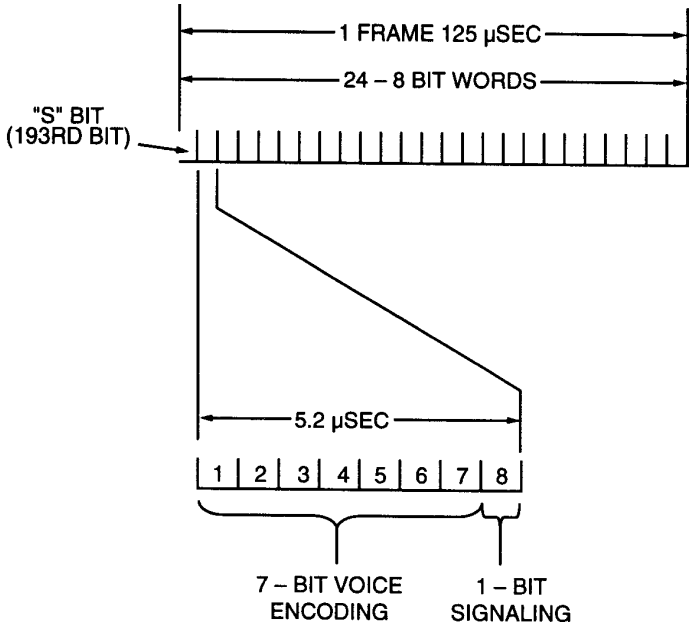


Figure 3–13. Word and frame.

Output rate. An additional bit time slot added to each frame (in 24-channel operation) is used to provide synchronization at the receiving multiplexer. This makes a total of 193 time slots per frame (24 channels x 8-bit code word plus 1-bit synchronizing slot). Multiplying the 193 time slots times the 8000-Hz sampling rate produces an output pulse train or output rate (R_o) with a bit rate of 1,544,000 bits per second. The clock period for a 24-channel multiplexer must be equal to the R_o (1.544 Mb/s), which is equal to 0.65 microseconds.

For 3-, 6-, and 12-channel modes of operation, an additional bit for synchronization is not used. The output rate (R_o) in the 3-, 6-, and 12-channel modes of operation is calculated by the following formula:

$$R_0 = (\text{number of channels}) \times (\text{sampling rate channel/sec}) \times (8 \text{ bits/sample})$$

Figure 3–14 shows the framing format for the 24-channel mode of operation. A group of 12 frames constitutes a *superframe.* Since each frame contains one synchronizing bit, the superframe contains a 12-bit sequence (identified as framing bits in fig. 3–14). This sequence is used for frame synchronization and for marking frame numbers 6 and 12, which contain signaling bits. This 12-bit sequence can be divided into two sequences: BF(t) (framing) and BF(s) (signaling framing). Framing bits BF(t) are odd-numbered, while BF(s) are even-numbered. The BF(t) bits alternate (1–0–1–0) every other frame. The receiver locates this sequence in the incoming bit stream to maintain or regain frame synchronization. Frame 6 occurs when the BF(s) bit is a 1 preceded by three BF(s) 1s, and frame 12 occurs when the BF(s) bit is a 0 preceded by three BF(s) 1s. The receiver detects this sequence to identify these two frames.

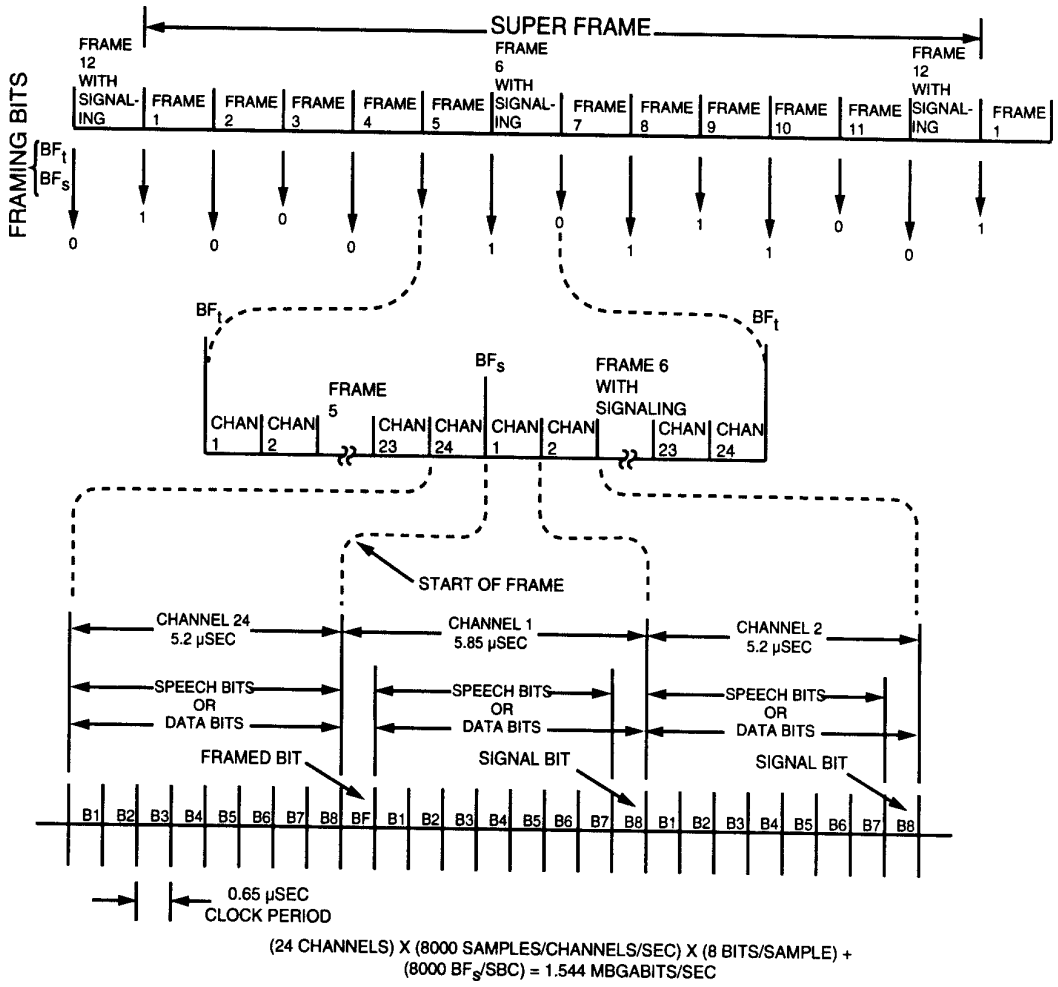


Figure 3–14. Framing format—24-channel mode.

The format for the 3-channel mode of operation is shown in figure 3–15. The superframe consists of 24 frames, each of which consists of three channel words. The channel words consist of 8 bits each, and the frame rate is 8000 frames per second. In this mode, no extra bandwidth is allocated to framing, since the framing bits are transmitted in B8 of channels 1, 2, and 3 during frames 12 and 24. Every 12th frame, the framing bits of channels 1, 2, and 3 is reversed, so that the 001 pattern appears to be followed by the 110 pattern 12 frames later. The signaling bits are transmitted in B8 for voice-only channels during frames 6 and 18. Each channel is transmitted as an 8-bit word for frames 1 through 5, 7 through 11, 13 through 17, and 19 through 23.

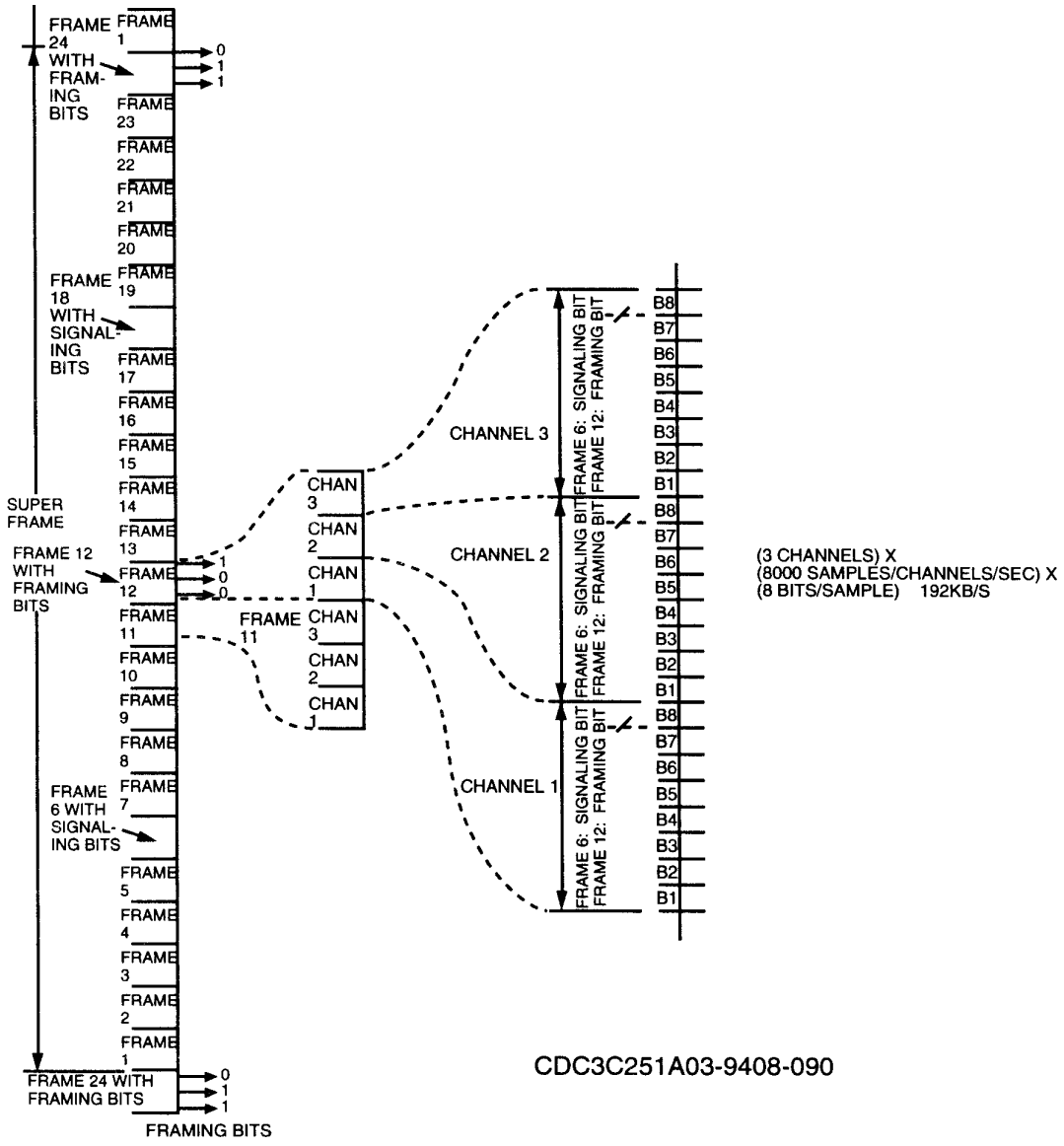


Figure 3–15. Framing format—3-channel mode.

The format for the 6-channel mode of operation is shown in figure 3–16. The superframe contains 24 frames, each of which contains 6 channels. The signaling and framing format is identical to that of the 3-channel mode, with signaling in B8 of each voice channel in frames 6 and 18 and framing in B8 of channels 1, 2, and 3 of frames 12 and 24.

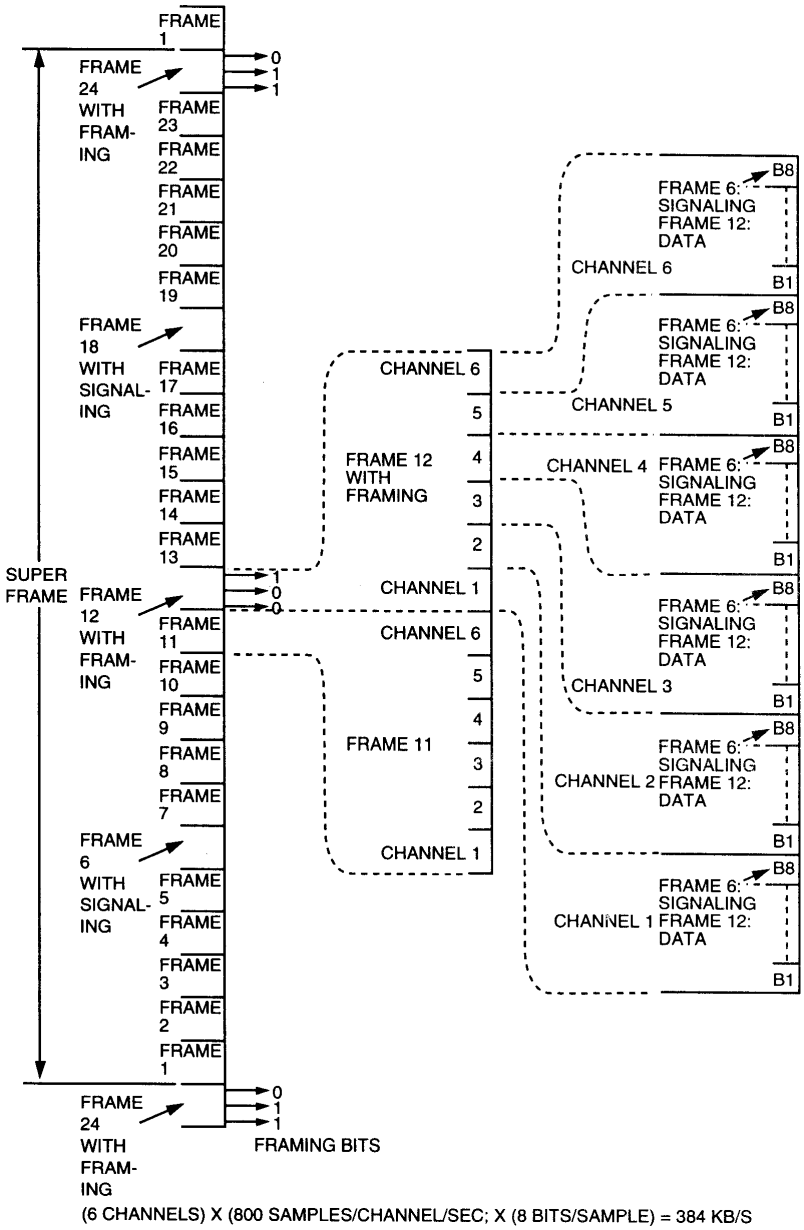


Figure 3–16. Framing format—6-channel mode.

The 12-channel frame format (fig. 3–17) follows directly from the 3-channel and 6-channel formats.

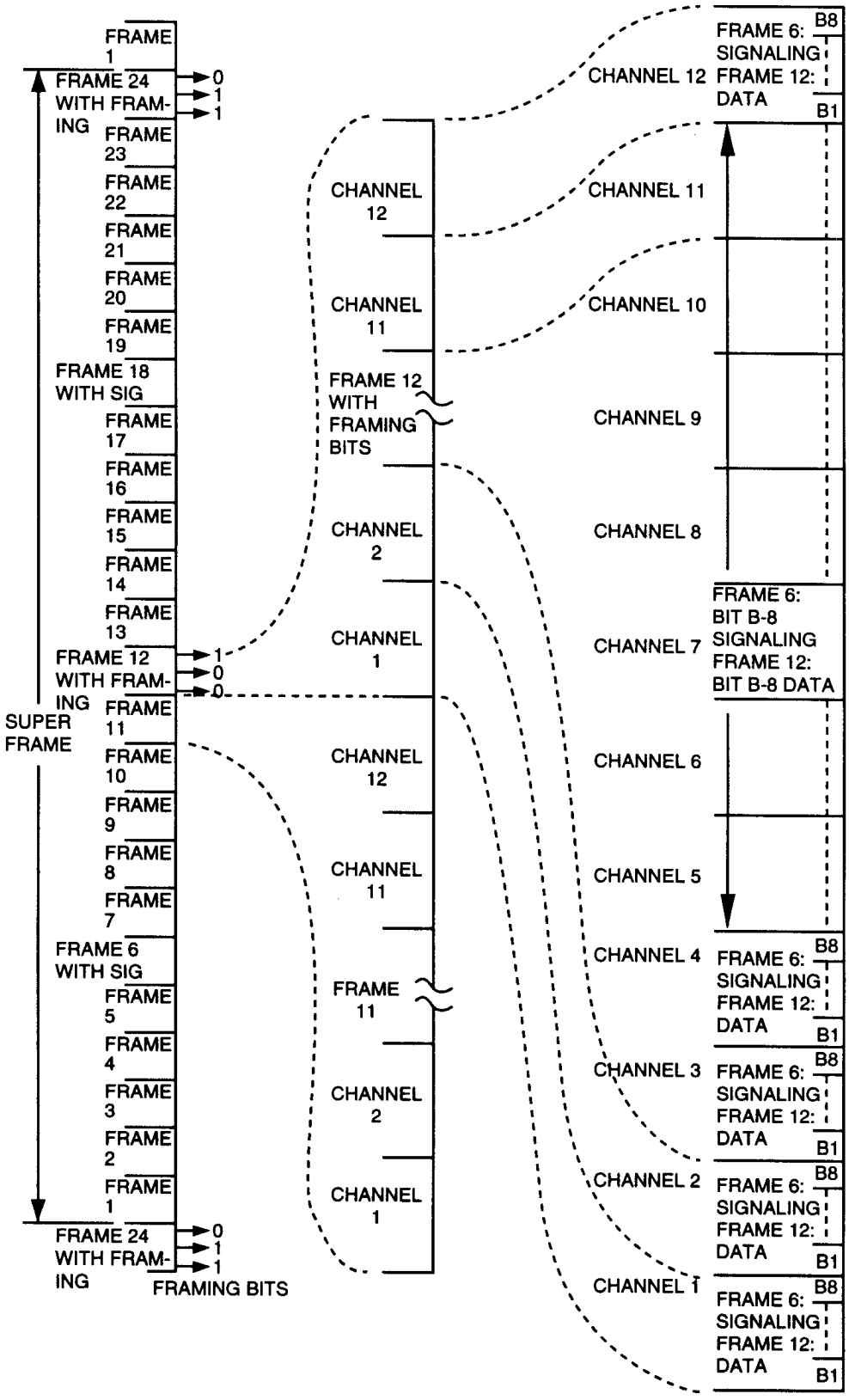


Figure 3–17. Framing format—12-channel mode.

Data processing. Each sample in the PCM pulse train is now in the form of an 8-bit non-return to zero (NRZ) word. The data is processed through an encryption device and then through an interface device in the AN/FCC–98. The interface device changes the NRZ data to bipolar data, which is used when the digital signal must be sent to another location for later processing. In most of our cases, when the data is to be locally processed, the signal remains in the NRZ form. The local clock is used to clock the data for further processing when it is fed to one channel of the AN/GSC–24 multiplexer in a satellite system or sent to a second-level multiplexer for further processing in telecommunications networks.

On the receive side of the AN/FCC–98, the process is reversed. The digital signal is decoded, and the original information is recovered.

The AN/FCC–99 multiplexer set is a duplex terminal with full transmit and receive capabilities. Each set is configured to specific communication system requirements by the installation of selected combinations of voice, data, and data timing interchangeable plug-in modules (fig. 3–18). Once the set is installed and operating in a communications system, it generally requires only scheduled preventive maintenance. If required, troubleshooting and corrective maintenance (module replacement) can be accomplished on-site while the set is in place.

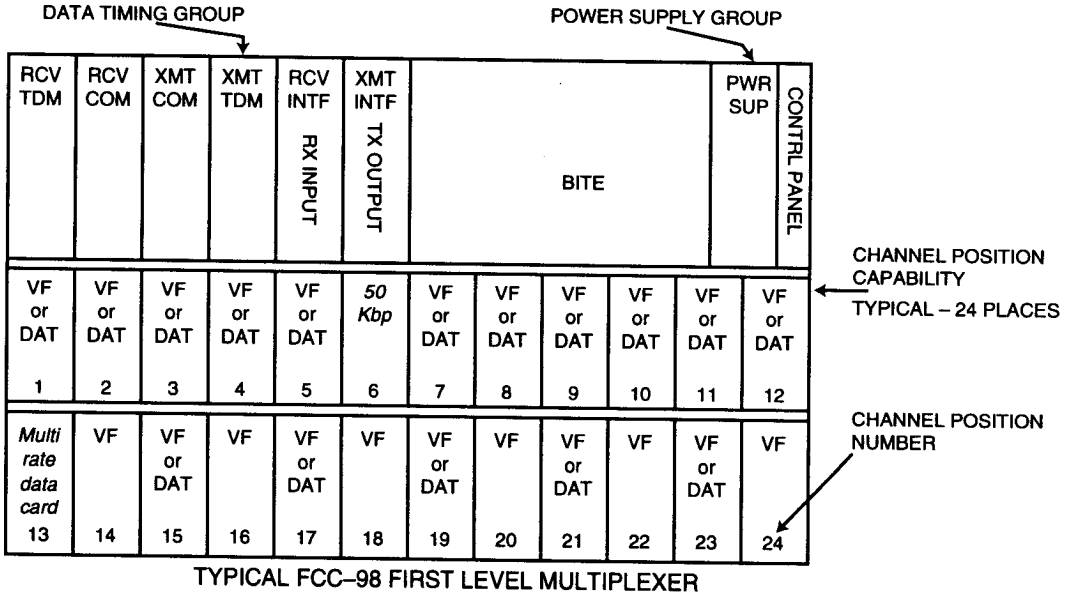


Figure 3–18. Typical AN/FCC–99 first-level multiplexer set.

Characteristics and functions of the second-level multiplexer

Basically, the second-level multiplexer multiplexes and demultiplexes from two to eight nonsynchronous T1 (1.544 Mb/s bipolar pulse stream) signals. This permits duplex transmission over a radio system capable of a flat bandpass of 400 kHz per T1 channel. Multiplexing the nonsynchronous T1 input signal is made possible by a technique known as pulse stuffing, which forces all inputs to a common synchronous bit rate of 1,544,935 b/s. The stuffed bits are removed at the receiving multiplexer with no degradation of the transmitted information. The bit rate of the inputs of 1.544 Mb/s is almost four times the flat bandpass required for transmission. The digital multiplexer is

able to operate with a narrower bandwidth by using three-level detection. Refer to foldout 3 at the end of this volume as we discuss the second-level multiplexer.

Conversion to NRZ from bipolar. The T1 input to the multiplexer is a 50-percent duty cycle, alternate bipolar pulse stream (fig. 3–19.) The stream contains 1,544,000 clock periods or bits per second. Information is carried by the presence or absence of pulses during the bit times. The presence of a pulse represents a logic 1 bit; the absence of a pulse represents a logic 0.

The multiplexer first converts the bipolar stream to unipolar. It then extracts a 1.544-MHz clock signal from the pulses and uses the clock to convert the stream to NRZ format. Notice that the NRZ signal changes level only when the corresponding bit value changes.

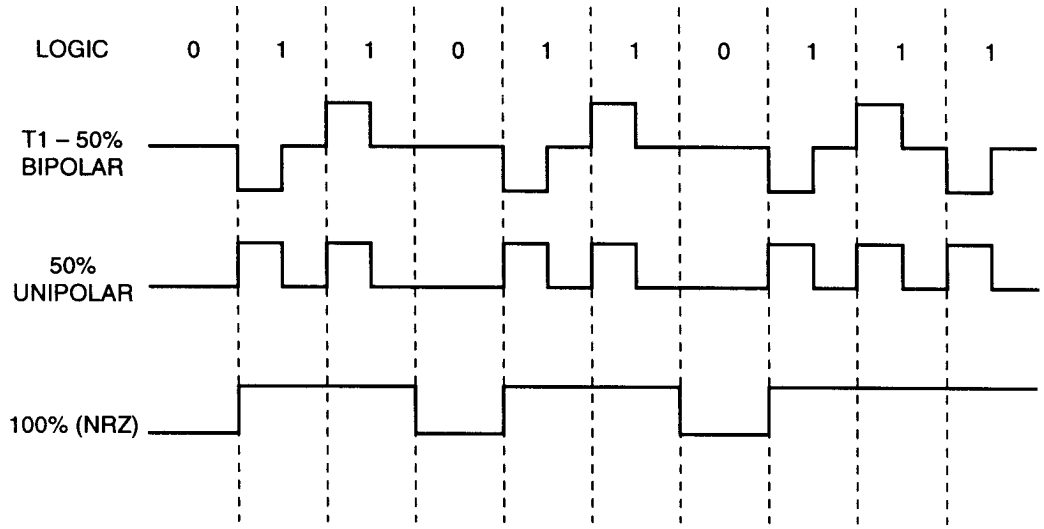


Figure 3–19. T1 and NRZ waveforms.

Stuffing. The information is loaded into the elastic storage at a rate of 1,544,150 b/s or less (fig. 3–20). It is unloaded at the rate of 1,544,935 b/s. The elastic storage accommodates this rate difference for a while, but not indefinitely. To ensure a continuous error-free operation under these conditions, a dummy bit must be inserted into the T1 stream. These dummy bits are called the *stuffed bits.* They do not contain useful information and are disregarded by the receiving multiplexer.

The reason for stuffing is to make sure that each stream contains exactly 1,544,935 b/s. A signal that is transmitted to the receiving multiplexer removes the stuffed bits.

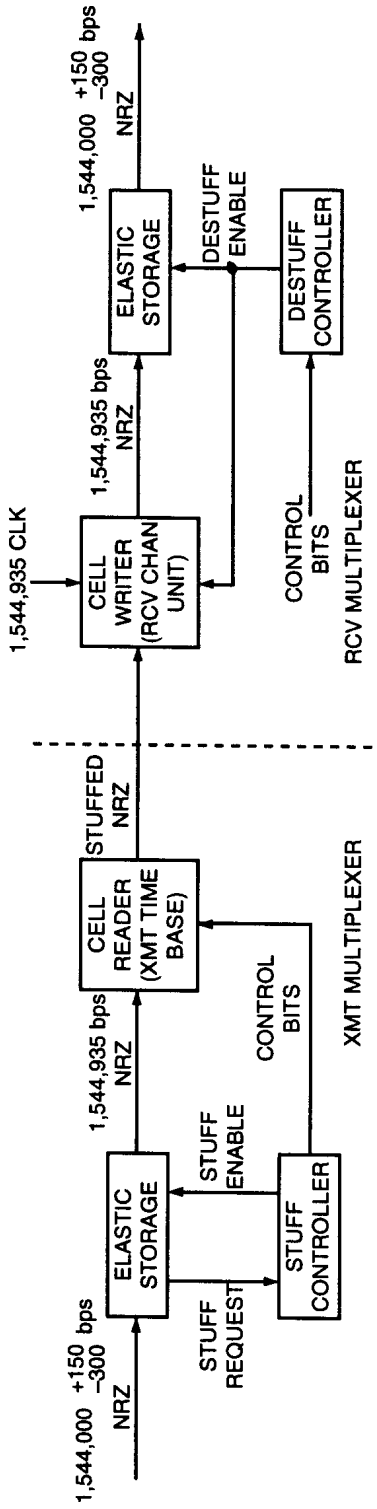


Figure 3–20. Stuffing and destuffing operation.

Multiplexing. The T1 signals from all the channels (8) are now fed through a sampling switch. The sampling switch looks through the input channels sequentially and breaks

them into timed segments. This signal is the time-division multiplex of all the channels. The signal is now divided into words. A “word” is made up of one bit for each T1 channel. (Notice that a T1 channel is also called a *port.*)

Frame organization. The words are organized into frames for transmission. In terminals consisting of more than 4 channels, the frame contains 16 words. The frame starts with a framing bit (BF) and, after 8 words, a control bit (BC) is added; 8 words later the frame is complete and another framing bit starts a second frame. For an 8-port second-level multiplexer, each word contains 8 samples.

The framing bits alternate between “1” and “0” (fig. 3–21).

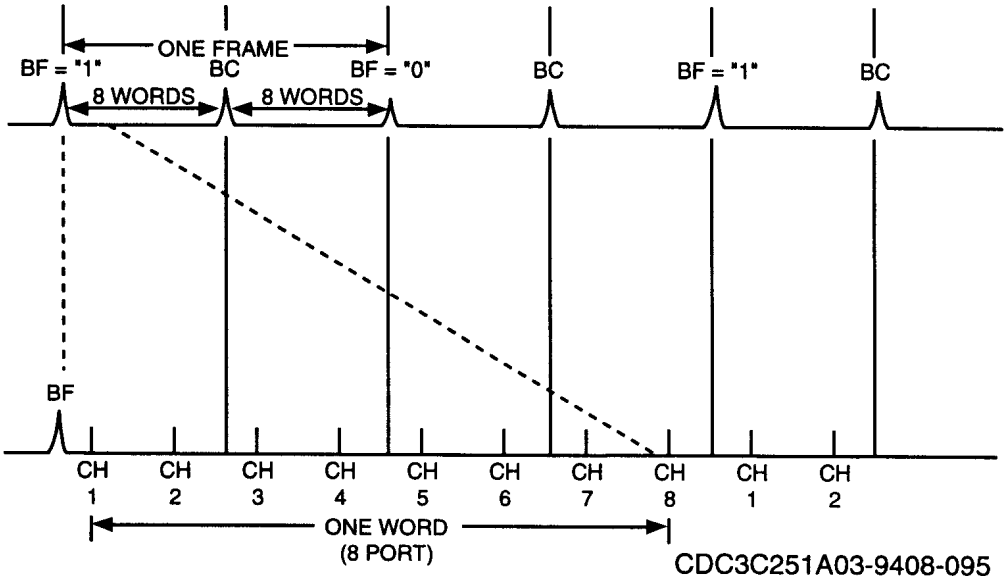


Figure 3–21. Framing and word format.

Scrambling. The multiplexed and framed signal (12.6 Mb/s) has all of the information needed by the receiving multiplexer, but it may not be suitable for transmission without one more step of processing. It is impossible to predict the data content of incoming T1 streams because it is possible that, at times, one or more of the T1 ports may not be supplied with a T1 stream. The 12.6-Mb/s stream may have large low-frequency components. Also, very few transitions are present in the data stream if all the T1 ports are inactive at one time. If this should occur, clock recovery would be very difficult at the receiving multiplexer. To ensure clock recovery and to remove the low-frequency components, the 12.6-Mb/s data stream is passed through a pseudo-random scrambler that eliminates the repetitive bit pattern and constant signal state by adding a pseudo-random word to the stream. It also ensures that the scrambled bit stream that arrives at the receiving multiplexer has a sufficient number of transitions for clock recovery.

Interface. The final step before transmission is interfacing. On the transmit side, the NRZ signal is adjusted to the proper level for the transmission facility and frequency. The signal is limited to the minimum bandwidth needed to carry the information content of the signal. By the use of three-level detection (figs. 3–22 and 3–23), the overall flat transmission bandwidth may be limited to one-fourth of the basic bit rate. For example, the 8-port terminal with a bit rate of 12.6 Mb/s requires a flat bandwidth (baseband) of

3.15 MHz at the 3-dB point. The three-level partial response waveform is produced by passing the NRZ bit stream through two low-pass filters, one before the transmission and one after it.

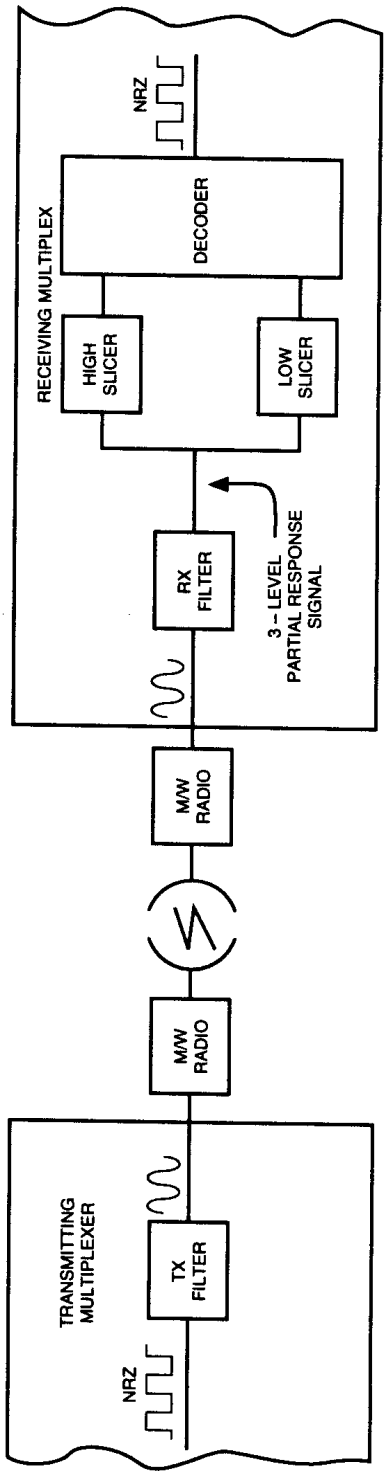


Figure 3–22. Three-level partial response block diagram.

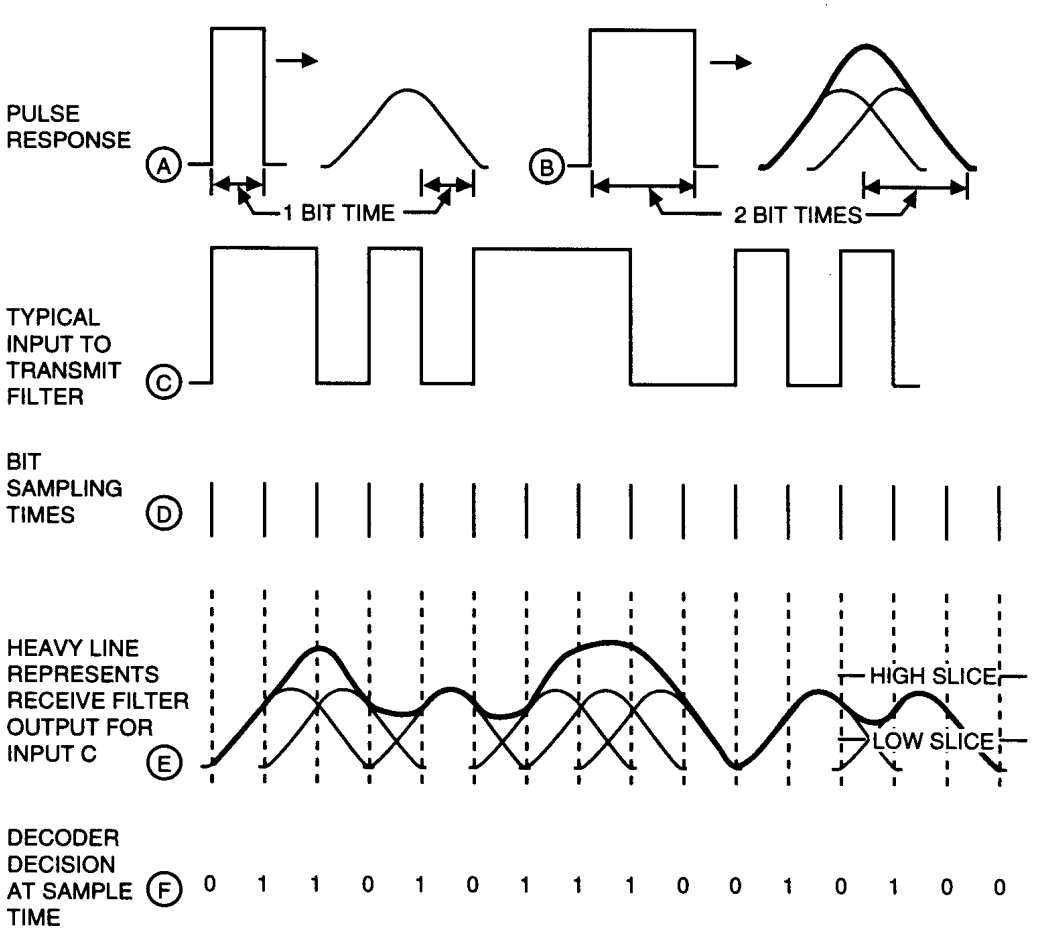


Figure 3–23. Response of combined filter characteristics.

Three-level partial response transmission is a technique that achieves the Nyquist sampling rate and deliberately generates and utilizes intersymbol interference as a means for producing a signal that has three distinguishable amplitude level ranges. The three ranges provide the basis for recovery of the input binary signal and reduce the bandwidth required for transmission to much less than that of a signal transmitted at two amplitude levels at the same rate.

The filtering before transmission is performed to begin rolling off frequencies above one-fourth of the bit rate being transmitted. This reduces the spectrum of the signal carried by the transmission medium to significantly less than that of a two-level signal at the same bit rate. Filtering after the transmission medium limits the incoming signal to frequencies present in the original waveform delivered to the transmission medium, removing any high-frequency noise added by the transmission medium. In addition to removing the high-frequency noise, this receive filter finishes the necessary shaping to produce the three-level partial response waveform.

Characteristics of the AN/FCC–99

The AN/FCC–99 multiplexer set provides second-level time-division multiplexing and demultiplexing of input/output (I/O) data between first-level and third-level communications equipment. Each set can be configured to operate with up to eight full-duplex first-level I/O ports in either a synchronous or asynchronous mode.

The multiplexer set (fig. 3–24) is a redundant time-division multiplexer/demultiplexer that can accept eight full-duplex non-return to zero (NRZ) or bipolar data inputs, each operating at a nominal data rate of 1.544 Mb/s. Operational configuration provides additional NRZ data rate options of 3.088 Mb/s per port and 6.176 Mb/s per port. The multiplexer operates in both the synchronous or asynchronous modes with any combination of port data rates whose combined rate does not exceed 12.352 Mb/s. Synchronous data is multiplexed into the Mission Bit Stream (MBS) using a fixed-rate conversion, while asynchronous data is multiplexed using positive bit stuffing. All inputs, with framing and overhead information, are multiplexed into a single serial output MBS. The multiplexer is operationally redundant with automatic, manual (local), and remote switchover (manual) capabilities.

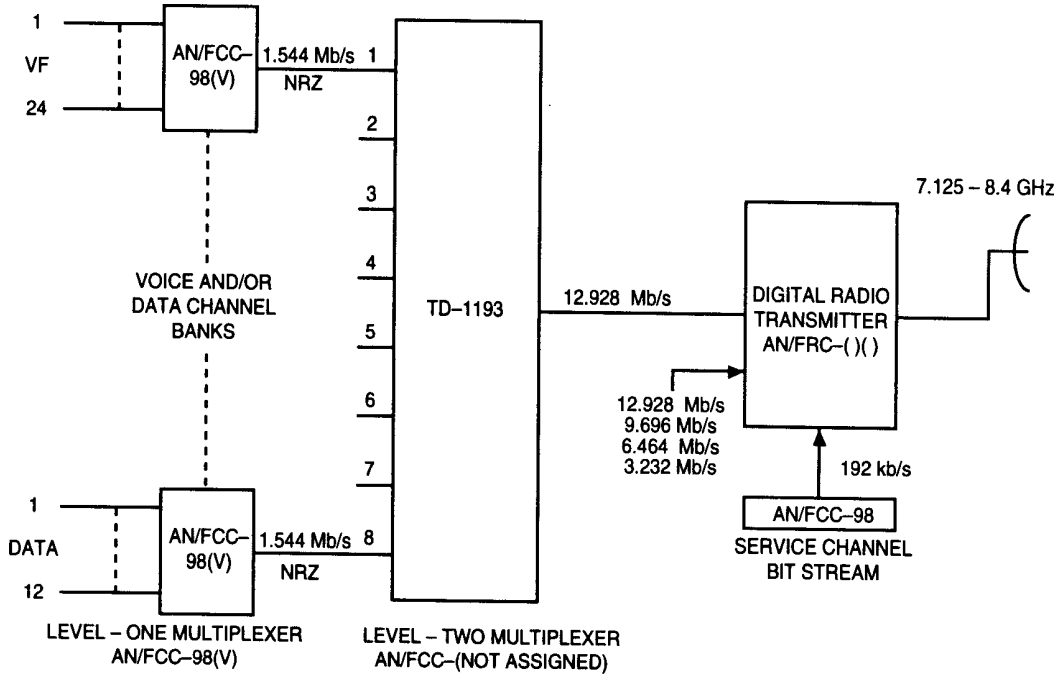


Figure 3–24. AN/FCC–99 multiplexer block diagram.

Data ports. The AN/FCC–99 can be easily configured to be compatible with different multiplexer sets (fig. 3–25) by using interchangeable port modules. Two types of interchangeable port modules (bipolar or NRZ) are used to configure the multiplexer set for various I/O interfaces. The bipolar port module operates at 1.544 Mb/s while the NRZ module provides port rate selection of 1.544, 3.088, or 6.176 Mb/s. The number of port modules and their individual data rates determine the multiplexer set MBS rate (3.232, 6.464, 9.696, or 12.928 Mb/s). The various

port rate combinations used to obtain the different MBS rates are shown in figure 3–26.

One characteristic of this multiplexer, along with others, is the fact that the port modules must always be arranged so that the port module with the highest selected port rate is installed in slot 1 with any additional port modules installed in order of the diminishing port rates. Also, if both NRZ and bipolar port modules are included in the same set, all bipolar port modules must be inserted to the left of the NRZ port modules.

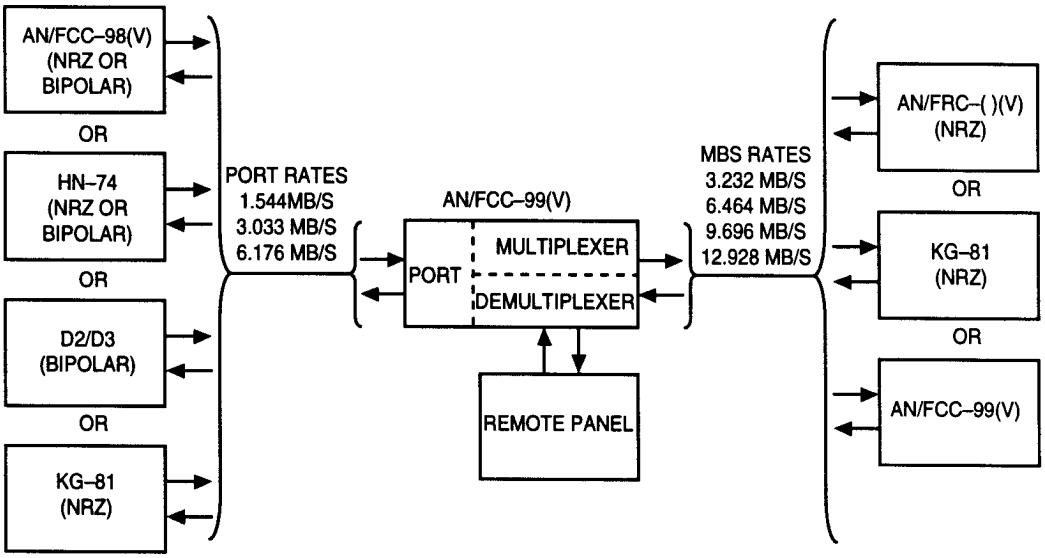


Figure 3–25. AN/FCC–99 second-level multiplexer in a digital network.

Port slots								Minimum MBS
1	2	3	4	5	6	7	8	rate
1.544								3.232
1.544	1.544							3.232
1.544	1.544	1.544						6.646
1.544	1.544	1.544	1.544					6.646
1.544	1.544	1.544	1.544	1.544				9.696
1.544	1.544	1.544	1.544	1.544	1.544			9.696
1.544	1.544	1.544	1.544	1.544	1.544	1.544		12.928
1.544	1.544	1.544	1.544	1.544	1.544	1.544	1.544	12.928
3.088								3.232
3.088	1.544							6.464
3.088	1.544	1.544						6.464
3.088	1.544	1.544	1.544					9.696
3.088	1.544	1.544	1.544	1.544				9.696
3.088	1.544	1.544	1.544	1.544	1.544			12.928
3.088	1.544	1.544	1.544	1.544	1.544	1.544		12.928
3.088	3.088							6.464
3.088	3.088	1.544						9.696
3.088	3.088	1.544	1.544					9.696
3.088	3.088	1.544	1.544	1.544				12.928
3.088	3.088	1.544	1.544	1.544	1.544			12.928
3.088	3.088	3.088						9.696
3.088	3.088	3.088	1.544					12.928
3.088	3.088	3.088	1.544	1.544				12.928
3.088	3.088	3.088	3.088					12.928
6.176								6.464
6.176	1.544							9.696
6.176	1.544	1.544						9.696
6.176	1.544	1.544	1.544					12.928
6.176	1.544	1.544	1.544	1.544				12.928
6.176	3.088							9.696
6.176	3.088	1.544						12.928
6.176	3.088	1.544	1.544					12.928
6.176	3.088	3.088						12.928
6.176	6.176							12.928

Figure 3–26. Port data rate combinations.

Multiplexing. The multiplexer module receives data from the transmit section of the port modules. Data transfer is based on a port polling system with the received data being written into a section within the transmit random access memory (RAM) of the multiplexer module corresponding to the appropriate port. A unique portion of memory is allocated for each port and the received data is sequentially written into that memory in 4-bit segments. The demultiplexer module demultiplexes received MBS data and writes the data into a receive RAM. A unique portion of memory is allocated for each port and the demultiplexed data is sequentially written into that memory in 4-bit segments as controlled by a sequencer.

The demultiplexer module demultiplexes received MBS data and writes the data into a receive RAM. The demultiplexer module continually monitors the MBS to detect a frame word and acquire frame synchronization. When frame synchronization is acquired, the sequencer provides correct sequencing of read/write operations. Data read out of the RAM is transferred to the receive section of the port modules in 8-bit segments. For asynchronous ports, the demultiplexer module also recognizes stuff codes and moves stuff data into the data queue.

Frame structure. The AN/FCC–99 transmits multiplexed MBS data and demultiplexes received MBS data using the framing structure shown in figure 3–27A and 3–27B. The mission bit stream is composed of superframes with each superframe consisting of up to eight frame pairs (even frame plus odd frame).

The number of frame pairs per superframe is dependent upon the MBS rate. Within each frame of a frame pair, there are eight subframes. The subframes contain the frame word for frame identification, the data, and possible stuff code and stuff data as applicable. Each frame contains 808 bits for a total of 1616 bits per frame pair.

To maintain a constant elastic storage level, the multiplexer module must transmit an average of 772 data bits per frame pair. This is accomplished in the synchronous mode by using a fixed-rate conversion and in the asynchronous mode by using positive bit stuffing. Within every even frame of the multiplexer output, four data bits are inserted into subframe 2 to ensure that a minimum average of 770 data bits is contained in each frame pair. During synchronous mode of operation, a stuff code is automatically generated in either the even or odd frame (initial selection is random with subsequent stuff codes occurring within the following similar frames). Four data bits are inserted into subframe 6. This ensures that the average transmission of data bits per frame pair is 772.

During the asynchronous mode, a stuff code is generated only as phase error is accumulated. The stuff data bits are then inserted as required into subframe 6 of the applicable frame. With bit stuffing occurring in both frames of a frame pair, the maximum average number of data bits which can be transmitted per frame pair is 774 (776 per even frame and 772 per odd frame).

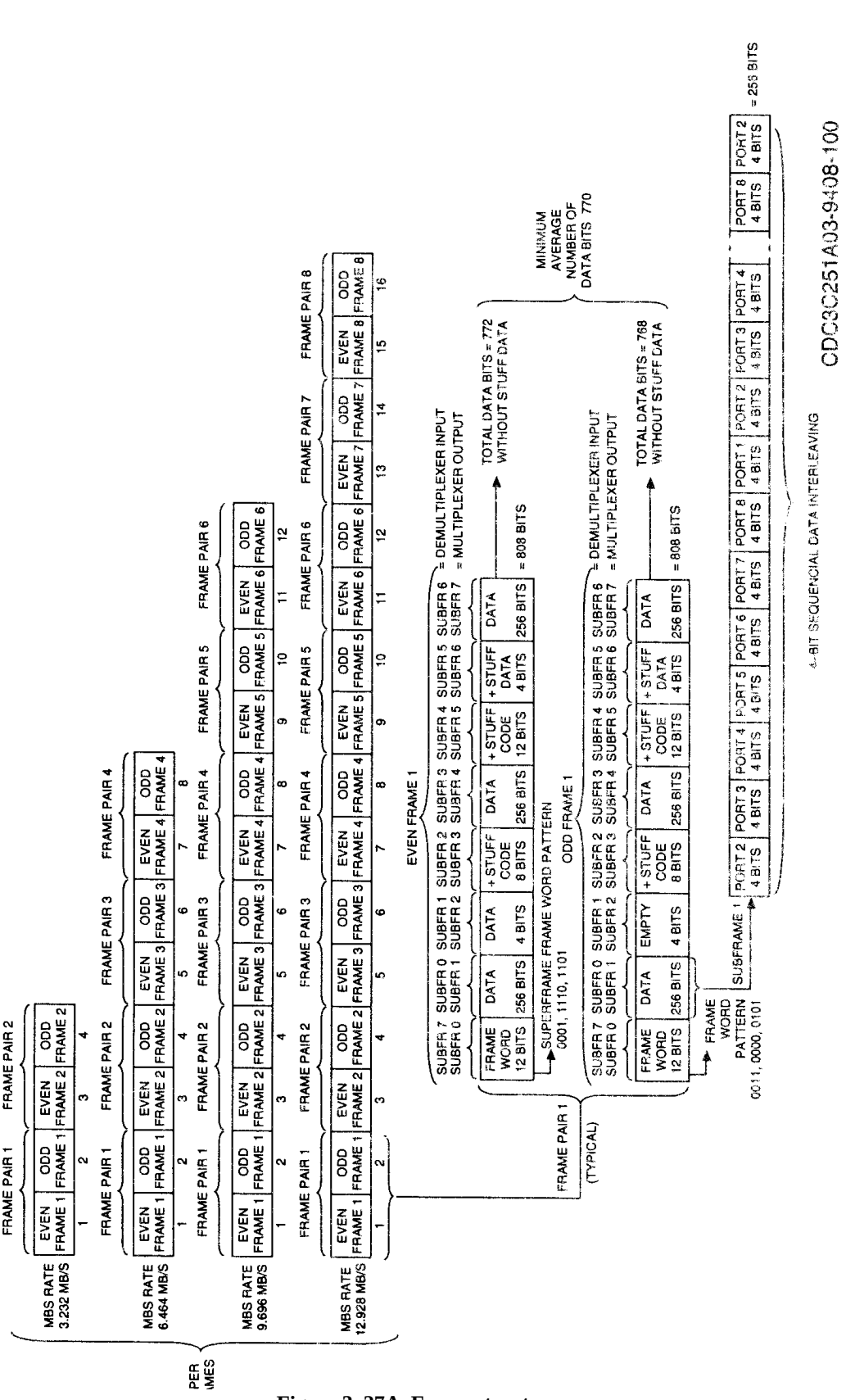


Figure 3–27A. Frame structure.

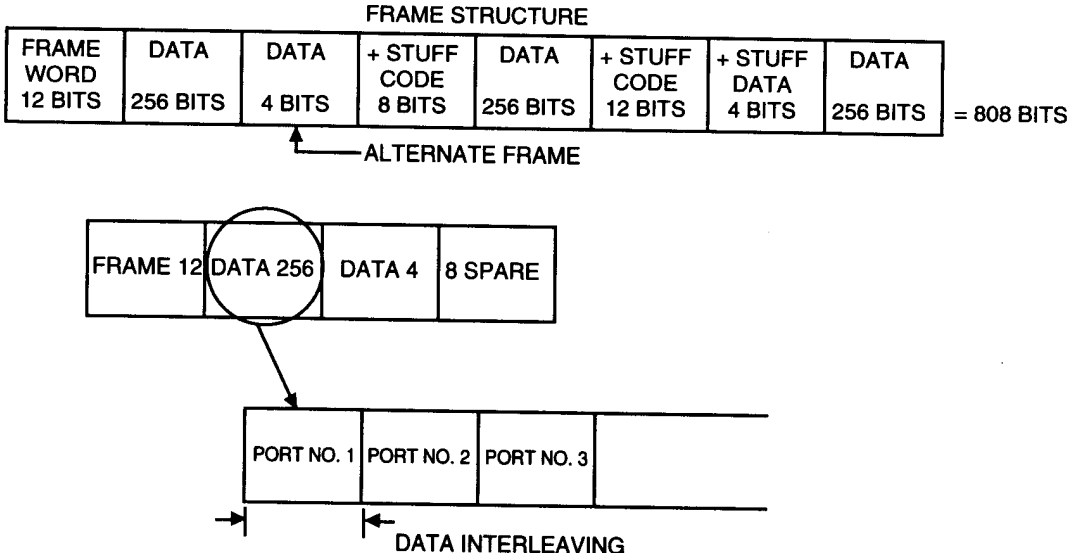


Figure 3–27B. Frame structure.

Bit stuffing is accomplished by associating each frame of a superframe with a particular port. The number of frames associated with a given port is a function of the port data rate. When the correct frame appears for a given port and the port requires bit stuffing, four bits are inserted into subframe 6 of the frame.

Since each frame is identical in structure, the demultiplexer module requires a method for associating each particular frame with its corresponding port. The superframe word identifies the beginning of a new superframe and provides synchronization for the demultiplexer frame counter. Each superframe begins sequencing at port 1. The frame counter can then identify the specific port to which a frame corresponds and determine if the present frame of the demultiplexer input is the even frame, which contains four bits of data in subframe 1.

System architecture. The operational design of the multiplexer set as used in the DRAMA system (fig. 3–28) is functionally divided into two sections: (1) I/O interfacing (port modules) and (2) data processing (multiplexer and demultiplexer modules).

A port receives the incoming data and clock and stores this data in temporary holding registers. After eight bits of data are received, the active port flags the multiplexer module to indicate that its holding register is full. The port module receives a data transfer acknowledge from the multiplexer module when data is transferred to the multiplexer data RAM. Similarly, the port module receives data from the demultiplexer module and transmits it, along with a smooth output clock, to the rear panel connectors of the multiplexer set.

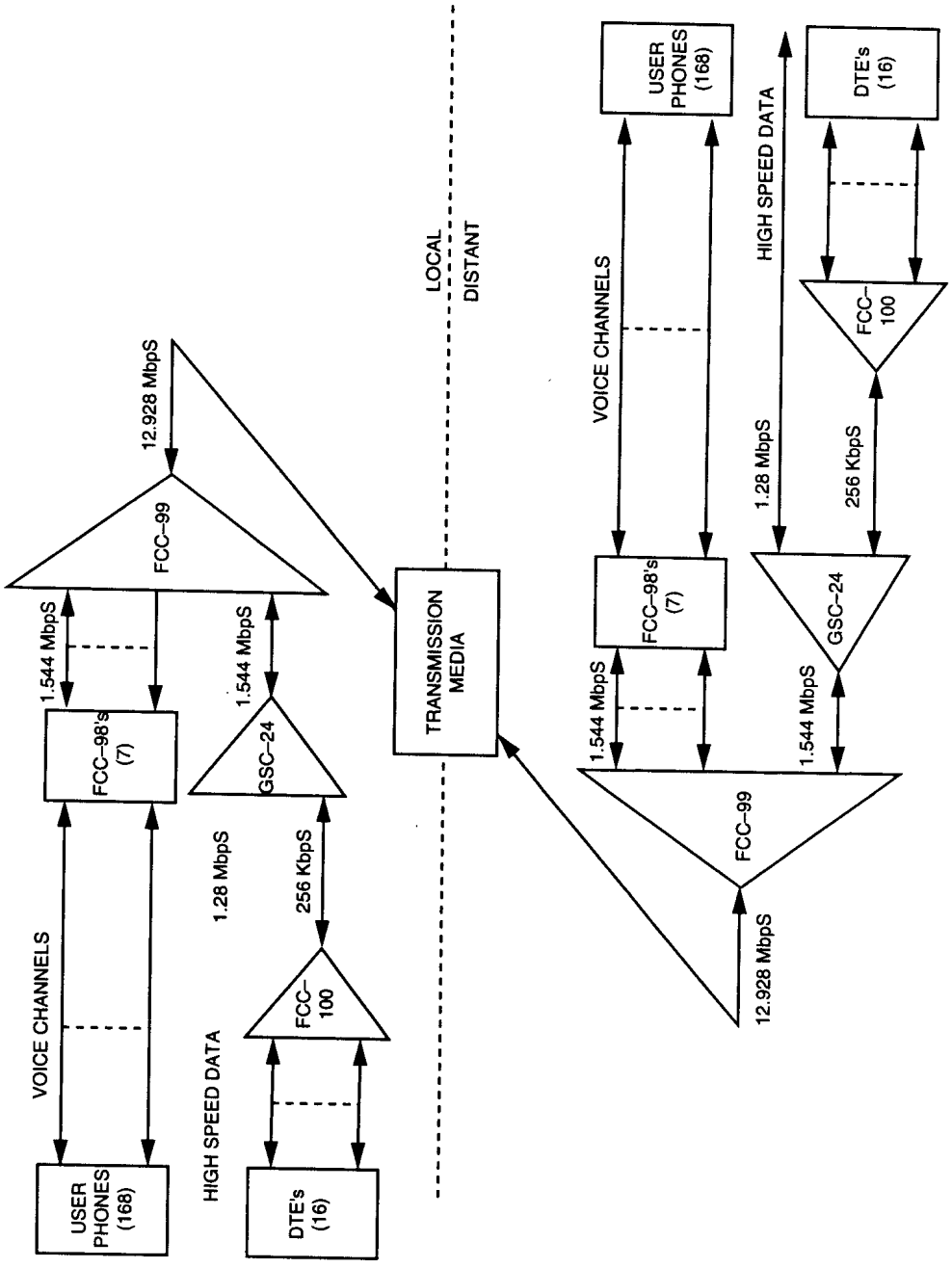


Figure 3–28. DRAMA simplified block diagram.

The multiplexer and demultiplexer modules continuously provide a smooth multiplexed and demultiplexed output stream while continuously monitoring port generator interrupt flags. The system clock for the multiplexer and demultiplexer modules is the MBS clock with each cycle being one MBS clock period. Two cycles are dedicated to moving data from the ports to the data RAM while the other two are dedicated to moving data from the RAM to the mission bit stream.

This concludes our discussion on modulation and multiplexing. We began with achieving a basic understanding of the various analog and digital techniques such as amplitude, frequency, phase and pulse modulation. Next, we applied this knowledge to comprehend the theory of multiplexing in its various forms (FDM and TDM). Finally, we completed our discussion by looking at some of multiplexing schemes employing these techniques and examples of equipment items used in the various multiplex stages.